Correction to "DiffRouter: A Differentiable Routing Framework for UltraScale FPGAs"

Xiaohan Gao*, Zhili Xiong*, Yusu Wang†, and David Z. Pan*
*Department of Electrical & Computer Engineering, The University of Texas at Austin, TX, USA
†Halıcıoğlu Data Science Institute, University of California, San Diego, CA, USA

This correction concerns the paper "DiffRouter: A Differentiable Routing Framework for UltraScale FPGAs," published in the proceedings of the 2026 IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), DOI: https://doi.org/10.1109/FCCM68464.2026.00029.

Description of the Correction

After publication, we identified an error in the auxiliary total-wirelength (**tot WL**) calculator used to generate the corresponding results in Table II. Total wirelength was reported in the paper as an additional routing-quality metric using a calculator adapted from the FPGA 2024 routing contest critical-path wirelength (**CPWL**) analyzer.

Specifically, FPGA 2024 contest does not provide offical total-wirelength analyzer. In the published implementation, certain local/non-INT routing resources that do not belong to the INT wire types were incorrectly assigned a unit wirelength cost of 1. Under the intended wirelength convention of FPGA 2024 contest, these resources should contribute 0. We corrected this issue by assigning the unit wirelength as 0.

In addition, the published Vivado total-wirelength values were obtained directly from Vivado design checkpoints (DCPs), whereas the other routers were evaluated from FPGA Interchange Physical Netlists. For the corrected evaluation, routed Vivado designs are first converted to FPGA Interchange Physical Netlists and are then evaluated by the same corrected calculator used for all other routers. This provides a uniform total-wirelength evaluation flow across all methods. We corrected the implementation and recomputed all total-wirelength results.

The correction affects only the reported total-wirelength values, their geometric-mean ratios, and text directly interpreting those values. The runtime and CPWL results are unchanged. The DiffRouter algorithm, experimental runtime results, CPWL results, and the principal conclusions of the paper are unchanged.

Correction to Table II

The runtime and CPWL columns of Table II are unchanged. The **tot WL** columns should be replaced by the following corrected values shown in Table I.

The geometric means are computed from per-benchmark ratios normalized to DiffRouter. The corrected results show that DiffRouter remains competitive in total wirelength relative to all the evaluated open-source routers; Vivado obtains a lower total-wirelength under the corrected and unified evaluation flow based on FPGA 2024 routing contest settings.

TABLE I
Corrected total-wirelength portion of Table II.

	tot WL ($\times 10^6$)				
Benchmark	Vivado [36]	RWRoute [18]	CUFR [22]	Potter [6]	DiffRouter
logicnets_jscl	0.412	0.499	0.510	0.580	0.501
boom_med_pb	1.384	1.884	1.782	1.968	1.719
vtr_mcml	1.419	1.668	1.659	1.832	1.651
rosetta_fd	-	1.858	1.834	2.029	1.850
corundum_25g	-	3.898	3.913	4.242	3.815
finn_radioml	1.350	1.536	1.545	1.772	1.545
vtr_lu64peeng	2.675	3.049	3.081	3.458	3.061
corescore_500	1.957	2.220	2.218	2.606	2.248
corescore_500_pb	2.621	3.318	3.379	3.643	3.224
mlcad_d181_lefttwo3rds	8.757	10.346	9.888	10.634	9.791
koios_dla_like_large	7.077	7.467	7.507	8.188	7.455
boom_soc	7.562	9.168	9.151	10.302	9.080
ispd16_example2	8.621	10.062	10.159	11.261	10.048
rapidwright_picoblazearray	1.871	1.951	1.934	2.207	1.962
corundum_100g	-	4.253	4.272	4.640	4.205
koios_clstm_like_large	3.385	3.464	3.474	3.856	3.467
titan23_orig_gsm_x6	5.374	6.004	5.924	6.517	5.841
corescore_900	3.612	4.140	4.149	4.907	4.199
koios_dla_like_large_v2	8.683	9.086	9.057	9.815	9.053
finn_mobilenetv1	4.380	5.003	5.080	5.933	5.054
ispd16_fpga03	7.964	8.895	9.001	9.909	8.931
mlcad_d181	13.759	16.577	15.761	16.932	15.582
boom_soc_v2	9.984	12.799	12.431	13.422	12.071
corescore_1200	5.063	5.762	5.773	6.781	5.845
ispd16_example2_v2	7.517	8.666	8.726	9.719	8.646
corescore_1500	6.507	7.739	7.790	9.411	7.892
titan23_orig_dart_x4	6.849	8.115	8.181	9.185	8.004
corescore_1700	8.921	11.889	12.067	12.897	11.452
Geometric mean (ratio)	0.871	1.012	1.010	1.127	**1.000**

Correction to Section IV-B (Experimental Results)

The published paper states:

> "Overall, DiffRouter attains the best CPWL and tot WL among all baselines, demonstrating that our differentiable routing formulation ..."

The total-wirelength portion of this statement should be corrected. We propose replacing the sentence fragment above with the following neutral statement:

> "Overall, DiffRouter attains the best CPWL among the evaluated routers. The corrected total-wirelength results are reported in Table II."

Impact of the Correction

This correction changes the auxiliary total-wirelength statistics and the associated total-wirelength interpretation in Section IV. It does not change the routing algorithm, runtime measurements, CPWL measurements, or the main conclusions concerning DiffRouter's runtime improvement and competitive critical-path wirelength.