Floorplanning for Partially-Reconfigurable FPGAs via Feasible Placements Detection

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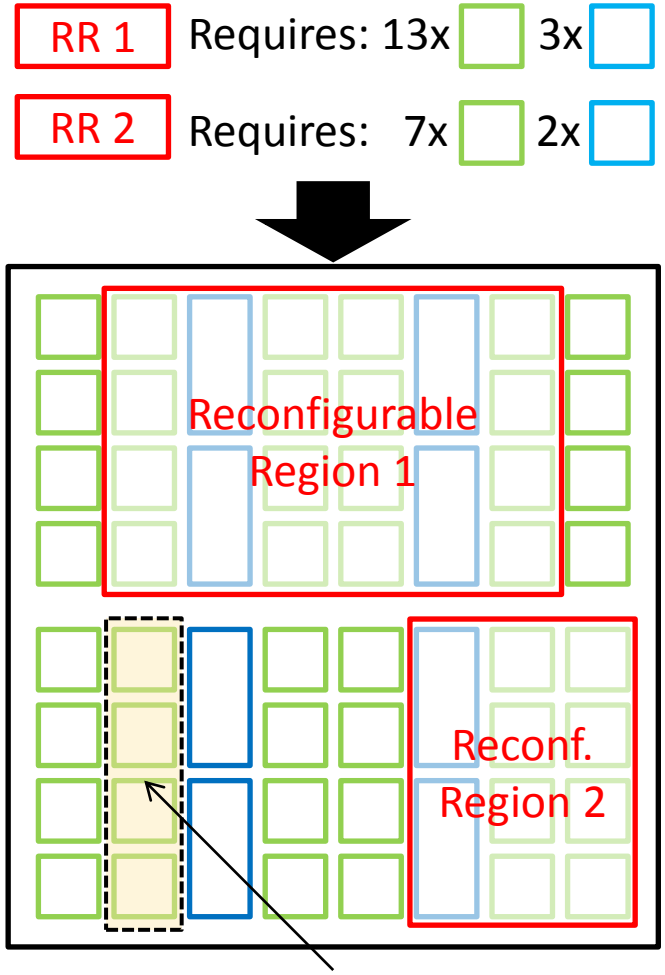
Rationale and Novelty

- Problem statement
  - Given a partially-reconfigurable FPGA, find on-chip area constraints to meet the design requirements

- Novelty:
  - Efficient exploration of the solution space driven by tight LP relaxations of the problem
  - Control on the shapes and positions of allowed areas
  - Possibility to customize the objective function by giving an arbitrary cost to each different area

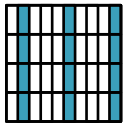
Floorplanning problem

- Given:
  - The FPGA description
  - A set N of reconfigurable regions (RRs)
  - The resource requirements $\forall n \in N$
- Goal:
  - Find a rectangular area for each region, such that:
    - No two regions overlap
    - Complete tiles are covered
    - All the resource requirements are met
    - A given objective function is optimized



Proposed Approach

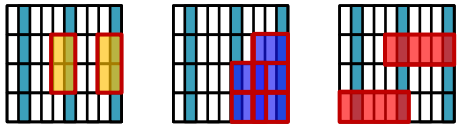
Reconfigurable regions +
Resource requirements



FPGA

Floorplan solution

Feasible placements generation



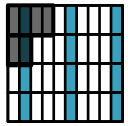
Possible regions placements

MILP model

$min\ c_1^t x + c_2^t y$

$x \in \mathbb{R}^{n_1}, y \in$

MILP Solver



Invalid and redundant placements

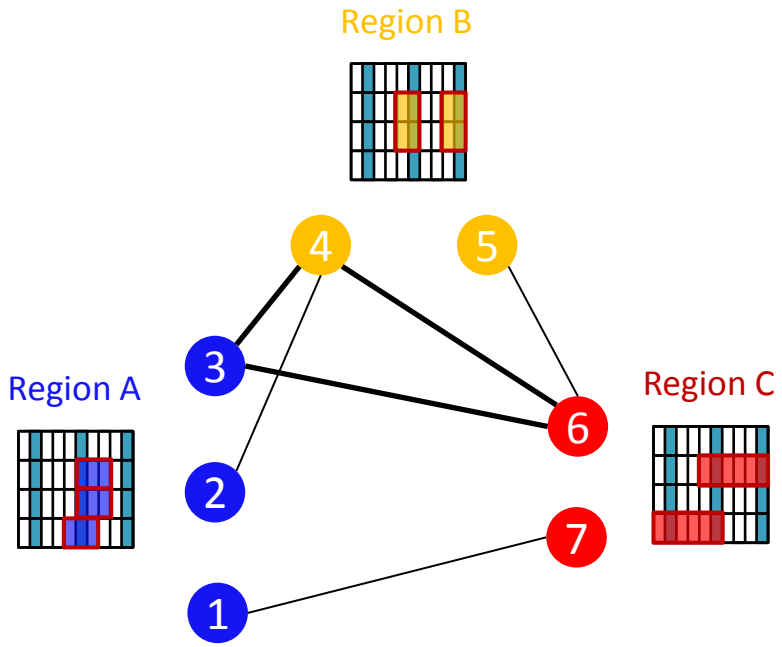
$min\ c_1^t x + c_2^t y$

User-defined linear Objective Function

MILP model overview

- Sets:
  - $\boldsymbol{N}$: set of regions (A, B, C)
  - $\boldsymbol{P_n}$: set of feasible placements for region $\boldsymbol{n}$ (P_A={1,2,3}, P_B={4,5}, P_C={6,7})
- Variables:
  - $\boldsymbol{x_{n,p}}$: binary variable set to 1 if and only if region $\boldsymbol{n}$ is assigned to placement $\boldsymbol{p}$
- Constraints:
  - No conflicting placements
  - One placement for each region

Placements conflict graph



$x_{A,1} + x_{C,7} \leq 1$

$x_{A,2} + x_{B,4} \leq 1$

$x_{B,5} + x_{C,6} \leq 1$

$x_{A,3} + x_{B,4} + x_{C,6} \leq 1$

Derived from a clique of size 3:
tighter formulation + constraints compaction

Benchmark results

- 20 designs with different number of regions and device occupancy rates to test the effectiveness of the proposed approach (PA)
- Global wire length objective function to compare to [1] and [2]
- MILP solver execution time limited to 1800 seconds

# RRs	Average wire length improvement w.r.t. [1]			Average execution time (sec)			
	HO[2]	O [2]	PA	[1]	HO [2]	O [2]	PA
5	6.99%	7.48%	7.46%	11.0	18.2	125.8	129.1
10	7.56%	12.05%	17.85%	24.1	111.5	1911.5	1803.7
15	8.83%	19.46%	31.59%	41.1	136.3	1936.4	1805.2
20	5.47%	19.98%	29.95%	65.5	123.0	1923.0	1806.4
25	5.52%	19.84%	38.11%	94.0	175.8	1975.8	1807.5

Occupancy	Average wire length improvement w.r.t. [1]			Average execution time (sec)			
	HO [2]	O [2]	PA	[1]	HO [2]	O [2]	PA
70%	8.44%	19.87%	28.61%	47.4	162.2	1633.2	1486.1
75%	5.49%	20.29%	25.43%	47.3	120.8	1568.5	1447.7
80%	6.20%	13.33%	25.89%	47.1	92.1	1553.6	1462.5
85%	7.36%	9.56%	20.04%	46.7	76.8	1542.7	1485.3

[1] Bolchini, C., Miele, A., and Sandionigi, C.: Automated Resource-Aware Floorplanning of Reconfigurable Areas in Partially-Reconfigurable FPGA Systems. In FPL, pages 532-538, 2011.
[2] Rabozzi, M., Lillis, J., and Santambrogio, M. D.: Floorplanning for Partially-Reconfigurable FPGA Systems via Mixed-Integer Linear Programming. In FCCM, pages 186-193, 2014.

THANK YOU!

FOR ADDITIONAL QUESTIONS CONTACT ME

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Feasible placements generation

- A placement **p** for region **n** is feasible if it covers all the resources required by region **n** and does not overlap with user defined invalid areas

- Placements generation strategies:
  - P_n: all feasible placements
    - Provable optimal solutions
    - High exploration cost
  - P_n^{irr}: irreducible placements
    - Provable optimal solutions for area minimization
    - Preserve problem feasibility
    - Low exploration cost
  - P_n^{w}: width-reduced placements
    - Suitable for wire length optimization
    - Medium exploration cost

Examples of feasible placements