Modular SRAM-based Binary Content-Addressable Memories

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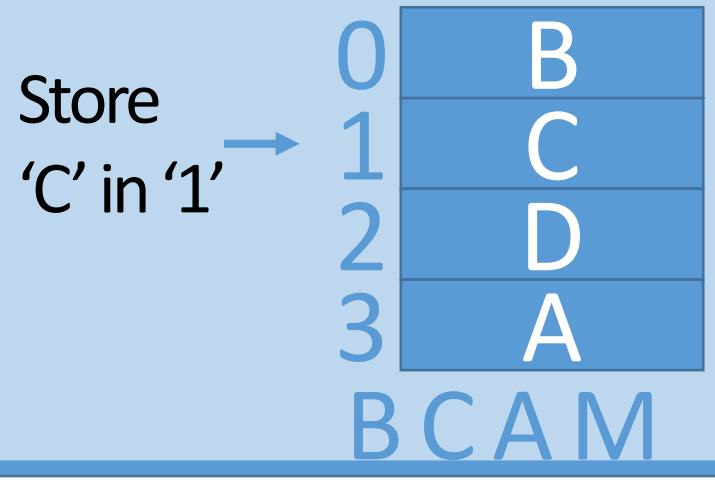
Vancouver, Canada

Binary Content-Addressable Memory (BCAM)

Hardware-based Single-Cycle Parallel Search Engines

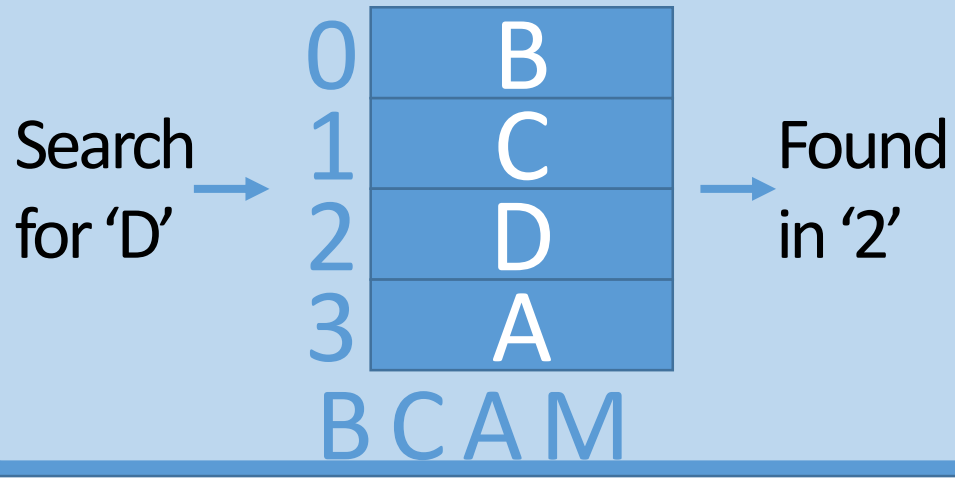
Write

Stores new data at specific address

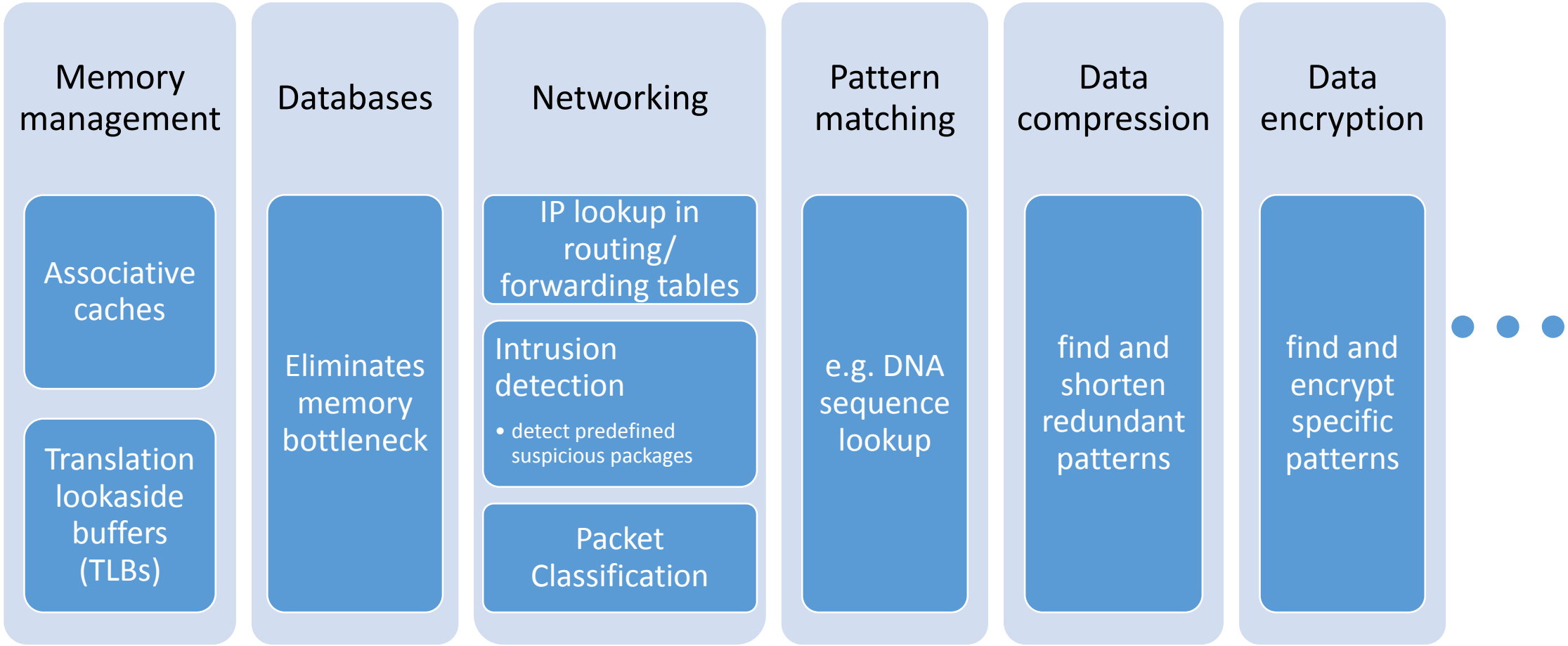


Match

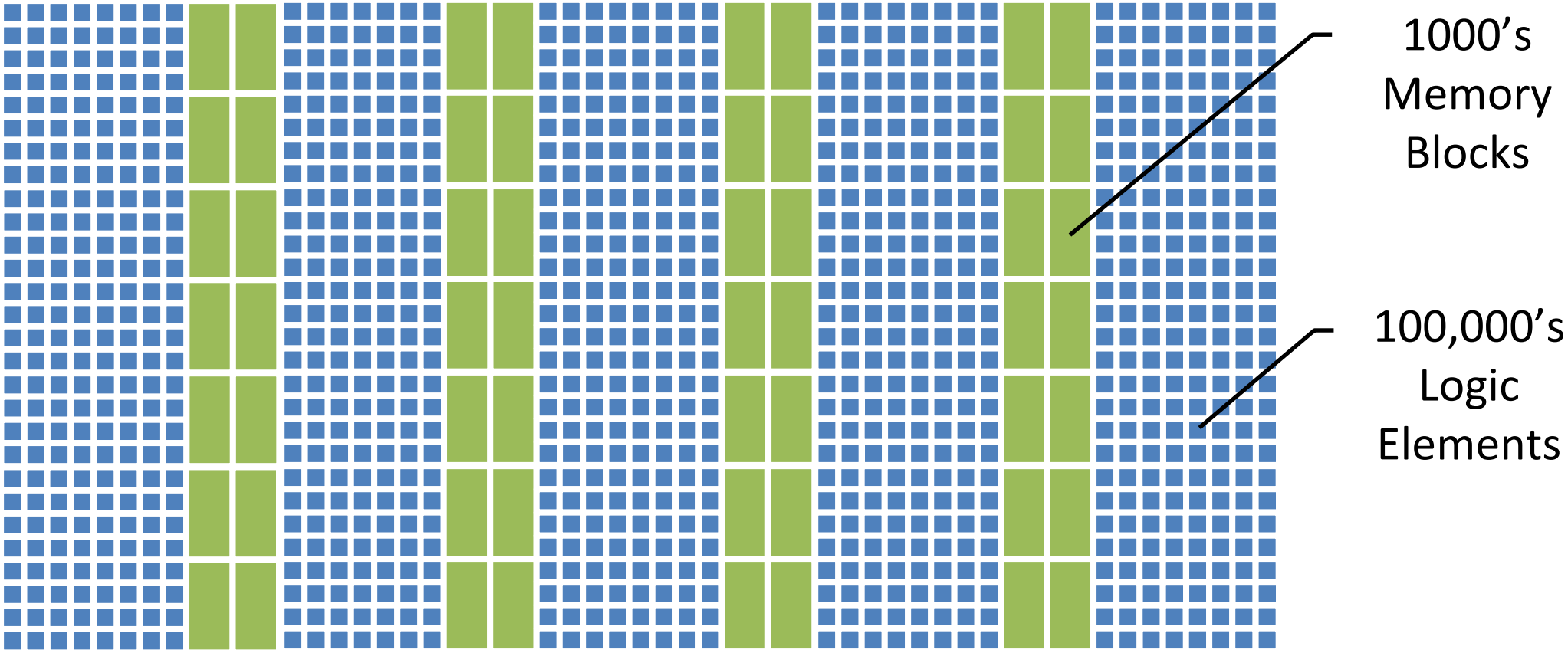
Search all addresses for a given data (pattern)



BCAM Applications



Motivation - FPGAs



No dedicated BCAM resources in FPGAs

Objectives

BCAMs

- Massively parallel memory search
- Require high memory bandwidth

FPGAs

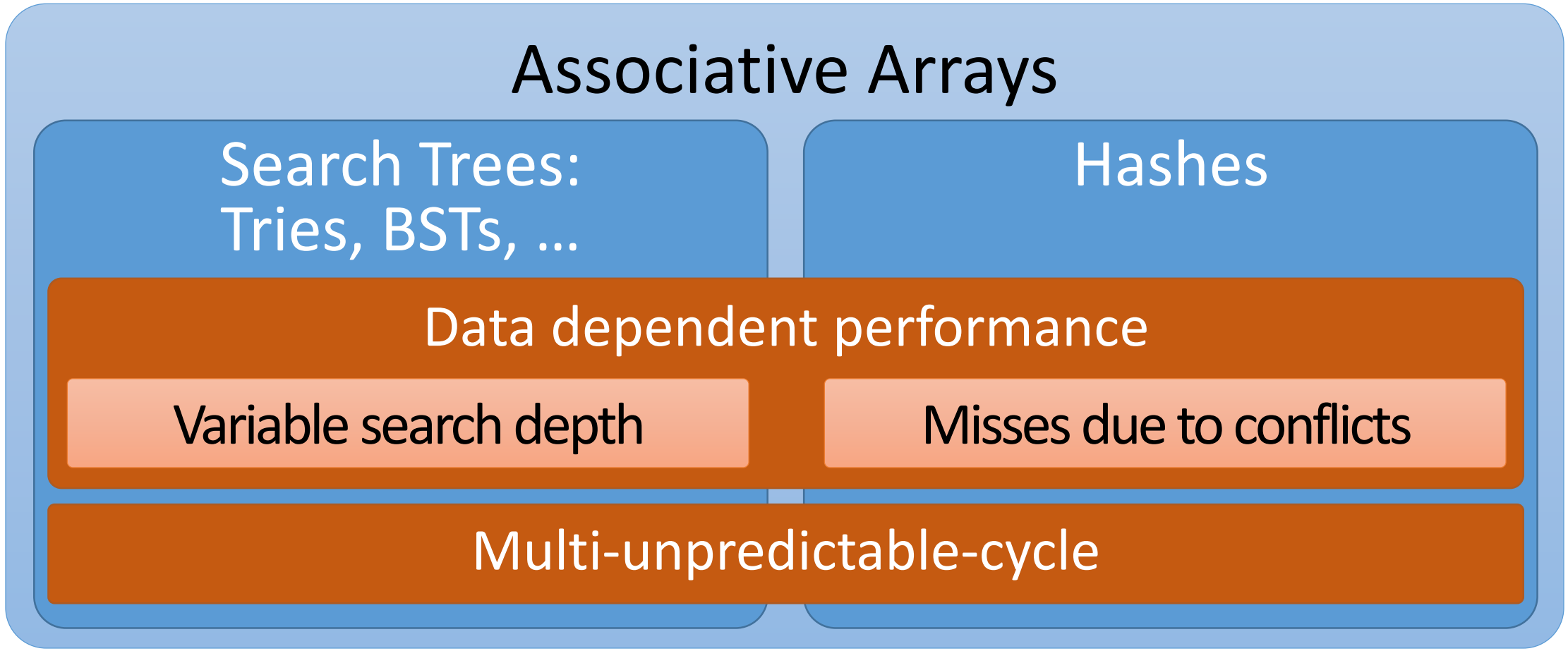
- Block RAMs are main storage
- Limited memory bandwidth

Use BRAMs to construct

- Modular and flexible
- Storage efficient
- Single-cycle
- Performance oriented

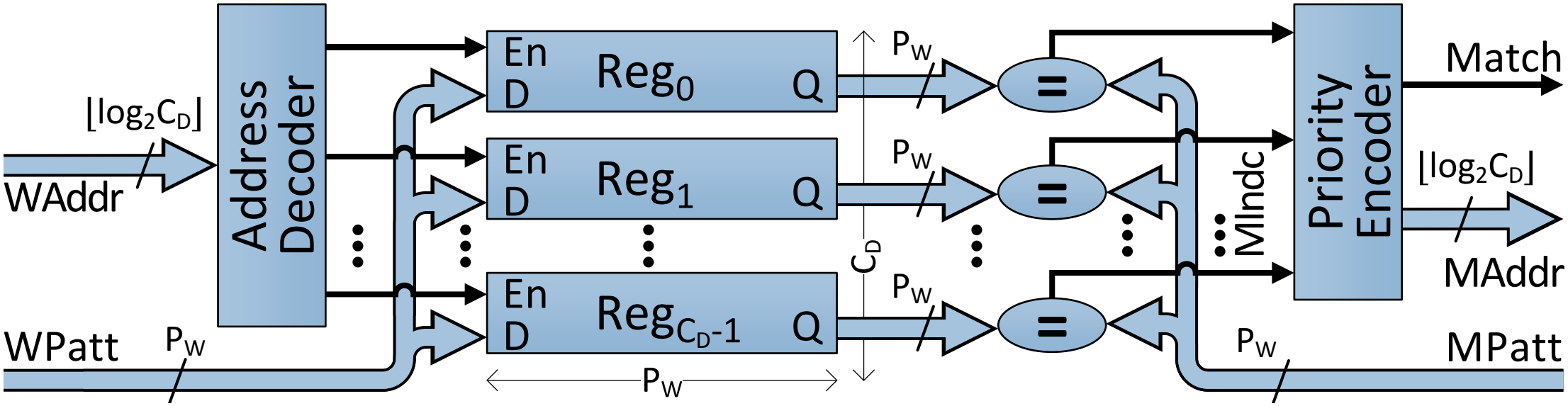
BCAMs

Algorithmic Heuristics



Register-Based BCAM

Concurrent register read and compare



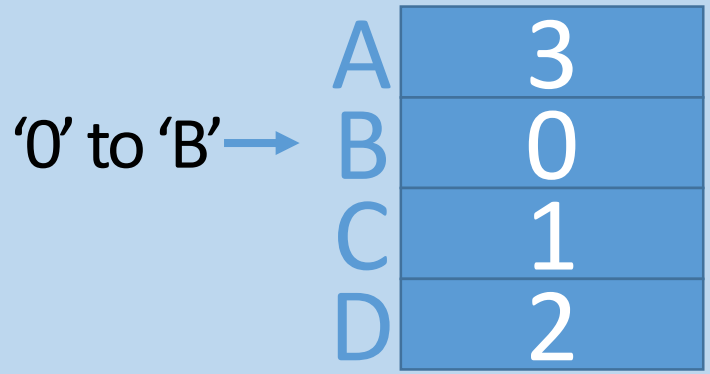
Single-cycle | **Limited resources** | **Complex routing** | **Fits small BCAMs**

Brute-Force Transposed-Indicators-RAM (1)
A Traditional BRAM-based BCAM

Key idea: Transposed RAM - data becomes addresses

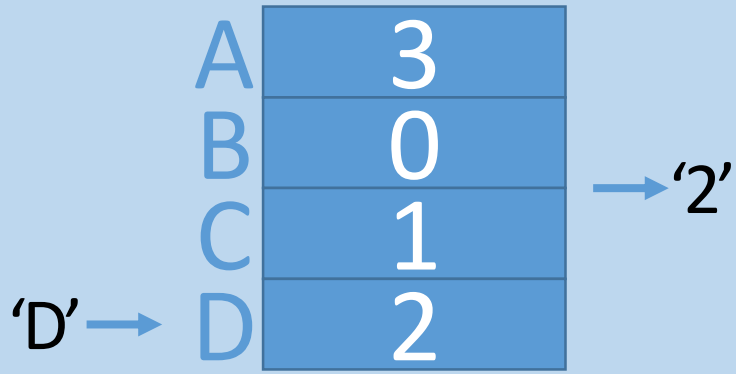
Write

Write ‘0’ to location ‘B’



Match

Read location ‘D’ for match



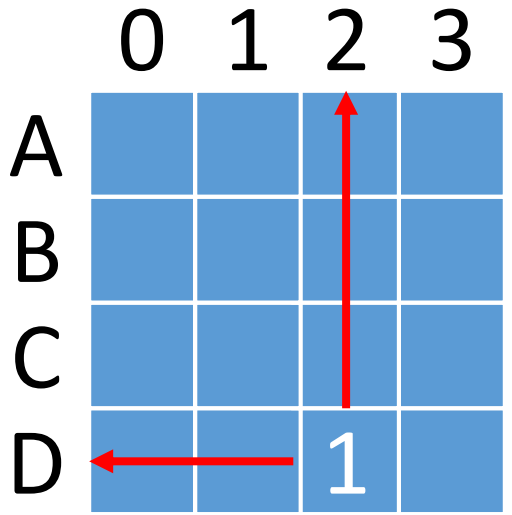
* Xilinx App Notes

Brute-Force Transposed-Indicators-RAM (2) Storing Data to Multiple Addresses

- How can we store data to multiple addresses?
  - Specify addresses using one-hot coding
  - Each bit indicates a match or “store at location”

➢PROBLEM: Depth of CAM is limited by data width of RAM

  - *e.g.* to build 1M deep CAM, we need 1M bits wide
  - In FPGAs: 1000 BRAMs x 32bit wide = 32K deep CAM



BRAM-based | Single-cycle | Depth of CAM is limited by RAM width

BCAM Cascading

- PROBLEM:
  - Patterns are encoded as RAM addresses

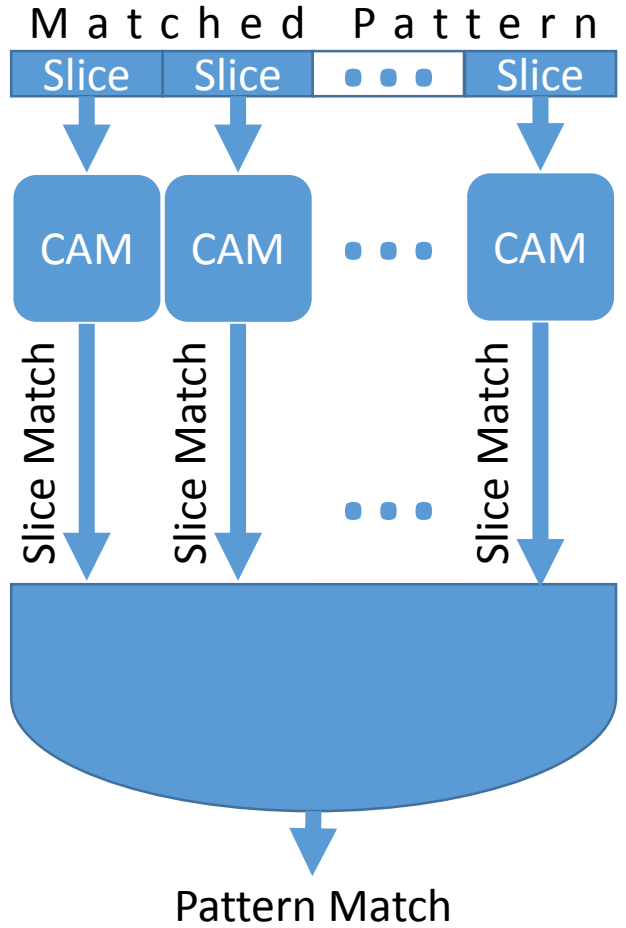
➢RAM depth is exponential to pattern width

$$\text{RAM Depth} = 2^{\text{Pattern Width}}$$

- Solution: Cascading
  1. Divide pattern into smaller slices
  2. Search for each slice separately
  3. If all slices are found → pattern match!

➢RAM depth is linear to pattern width

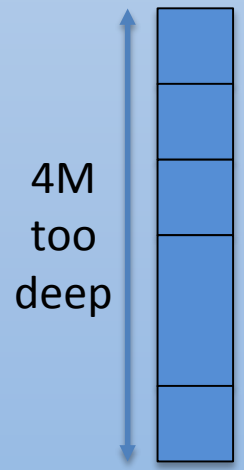
$$\text{RAM Depth} = 2^{\text{Slice Width}} \times (\text{Pattern Width} / \text{Slice Width})$$



Hierarchical Search 2D BCAM (1)
Narrow and Deep BCAM

Key idea: Hierarchical search

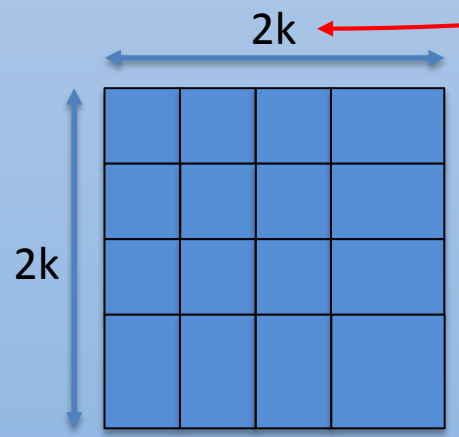
1D BCAM



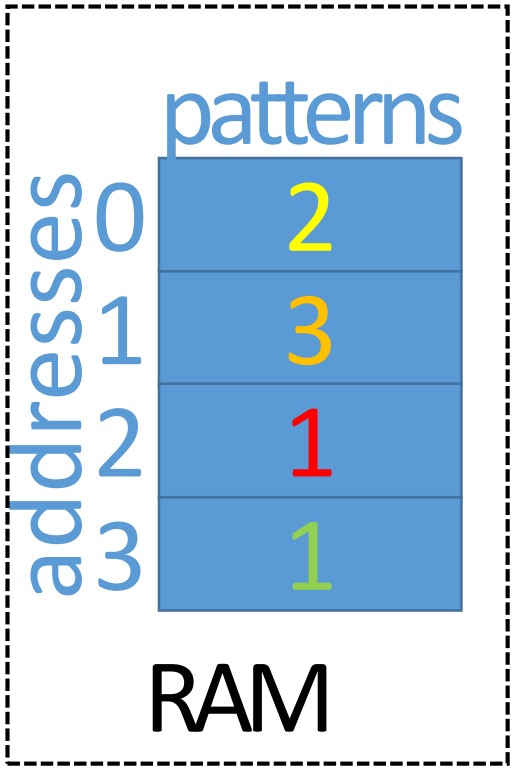
2D BCAM

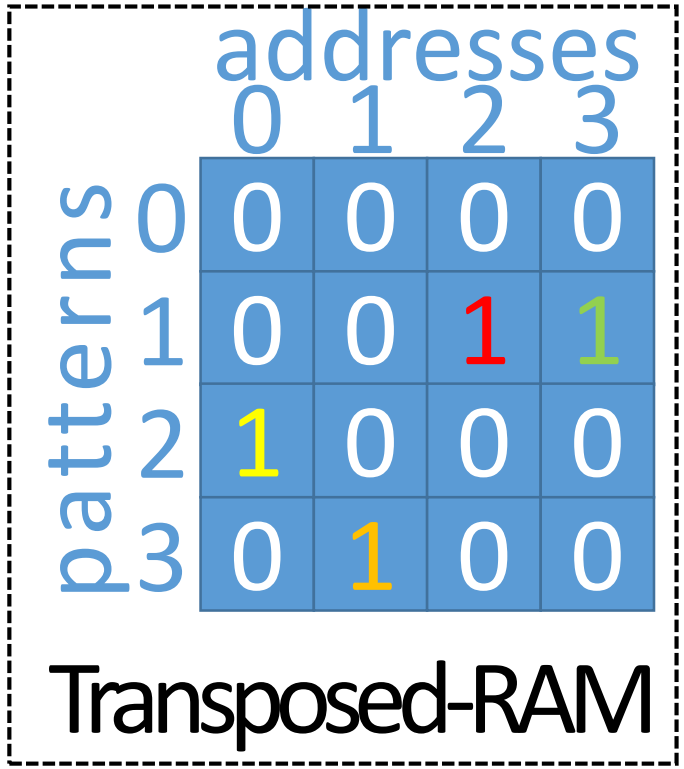
① Find a set (row) with match using a 1D BCAM

② Search this set (row) in parallel for a specific match



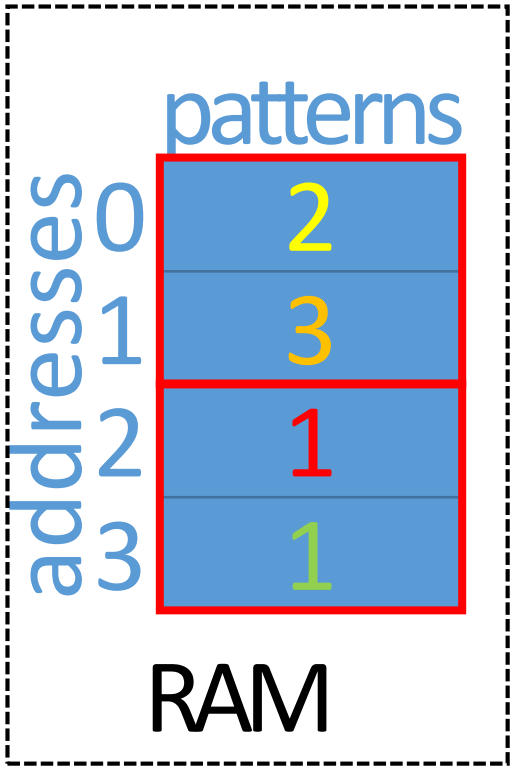
Hierarchical Search 2D BCAM (2) Example

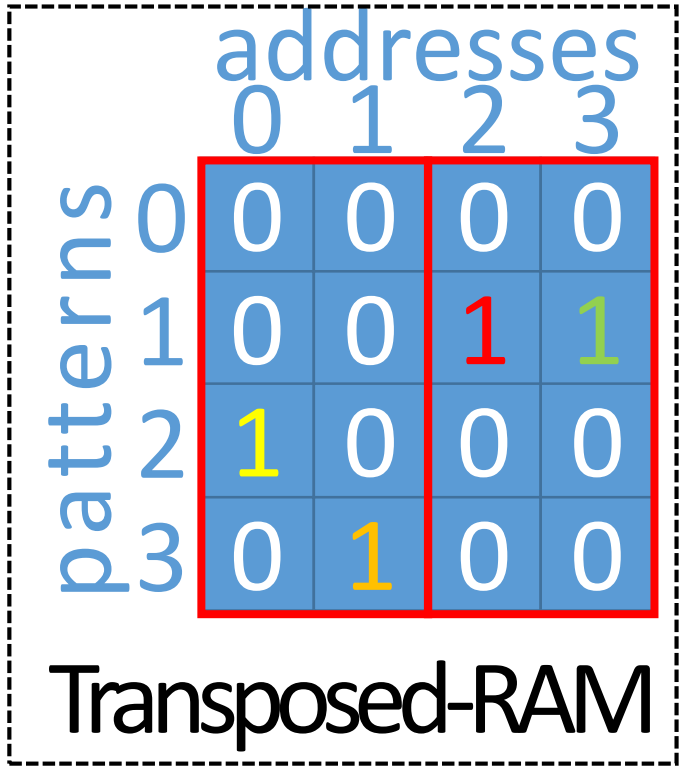




Hierarchical Search 2D BCAM (2) Example

- Divide address space into sets





Hierarchical Search 2D BCAM (2) Example

- Divide address space into sets
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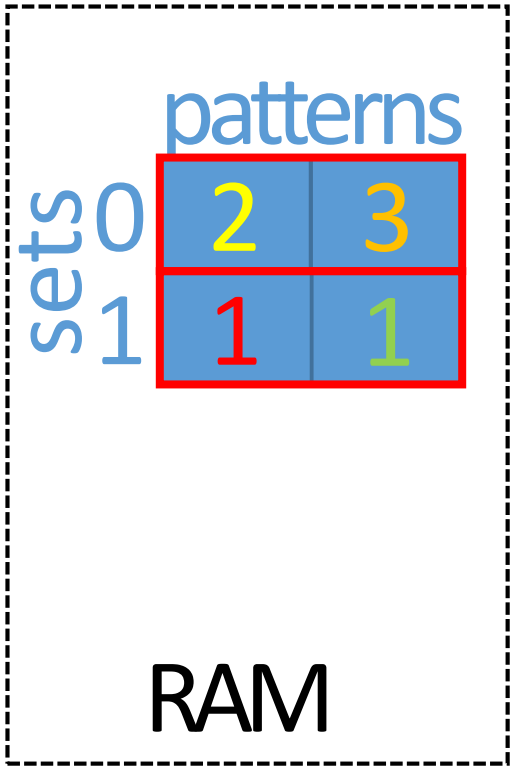

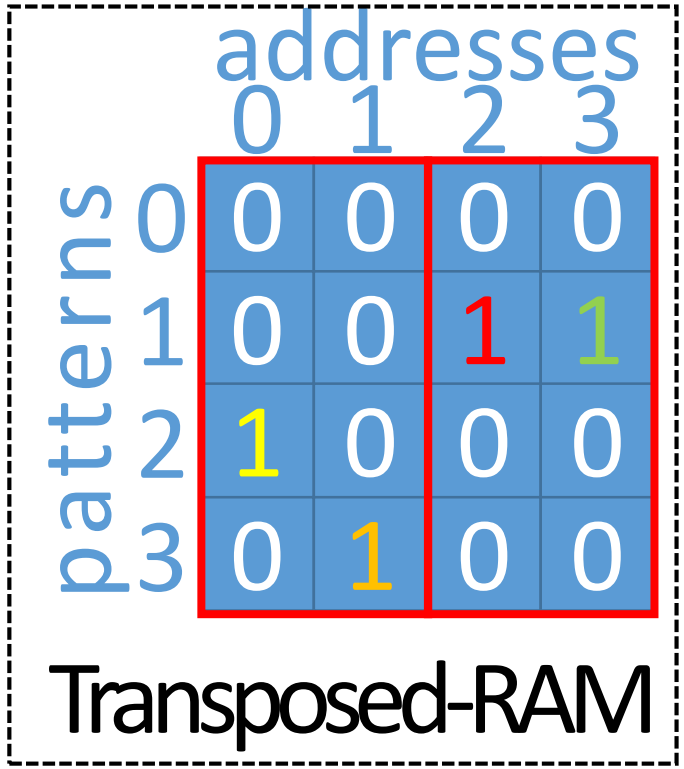

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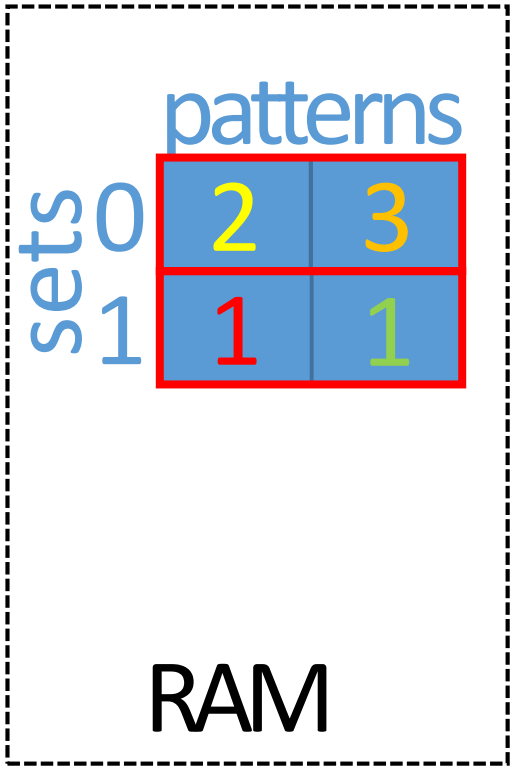

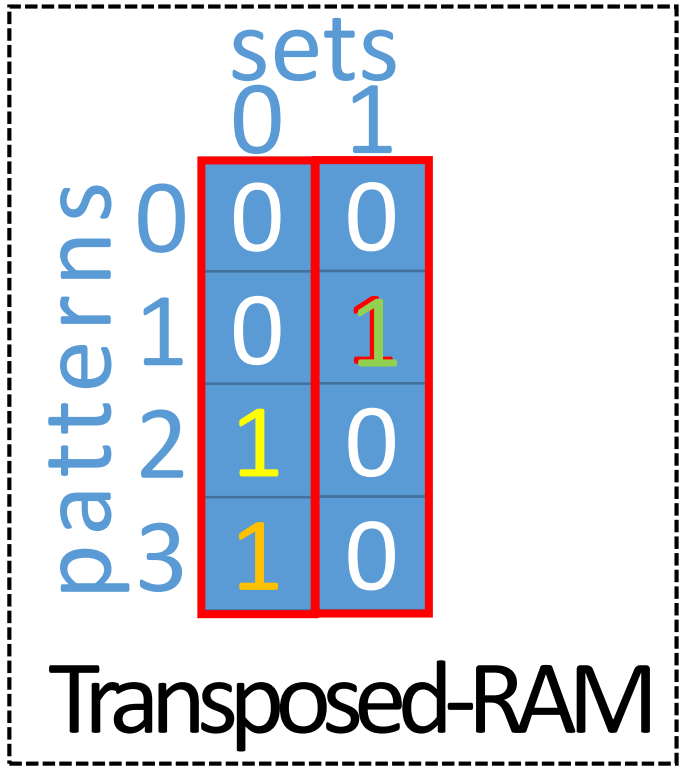

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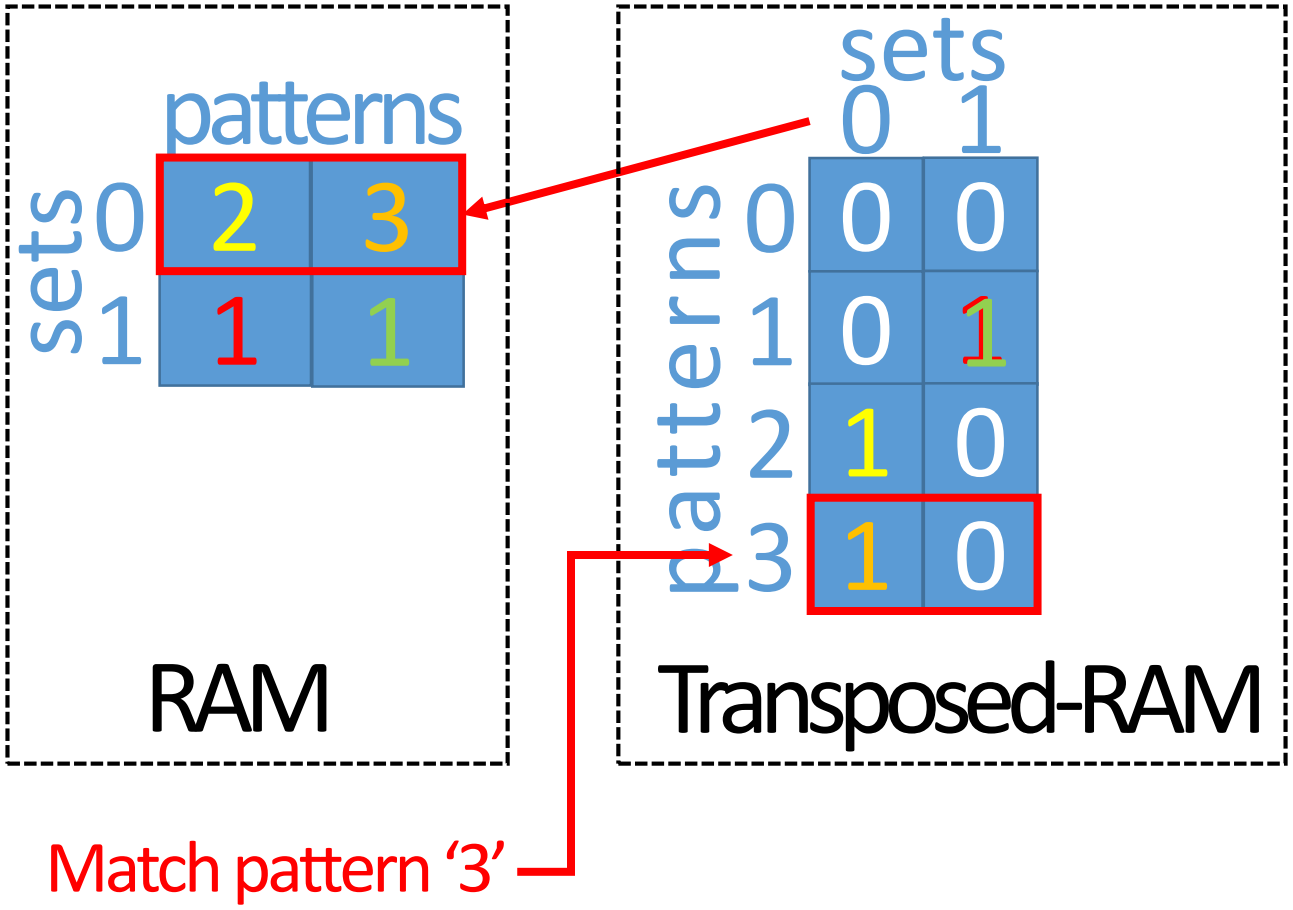

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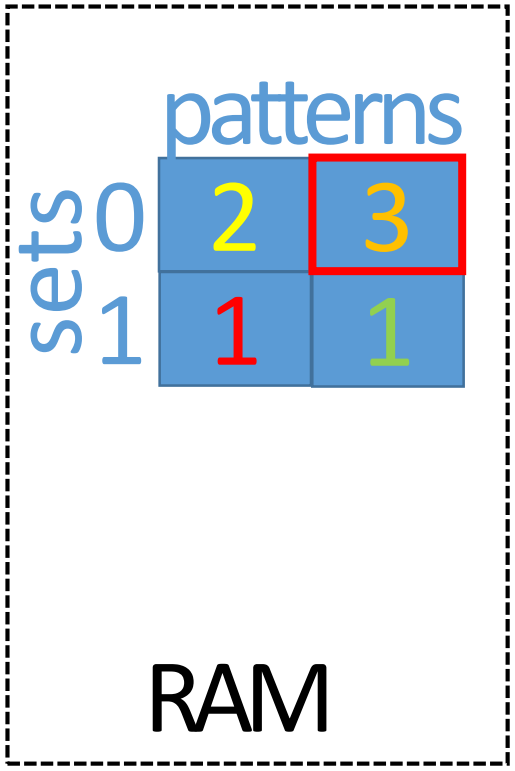

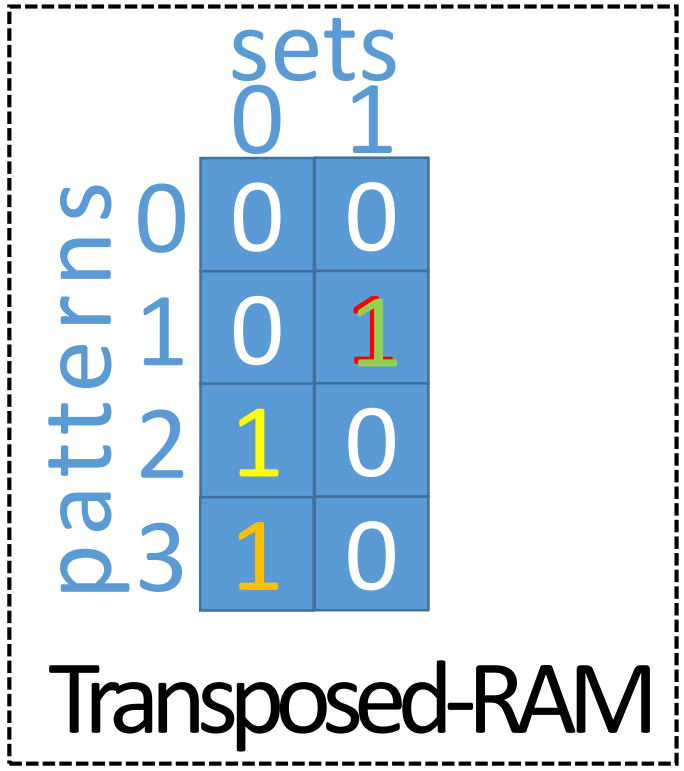

Hierarchical Search 2D BCAM (3)
Pros and Cons

BRAM-Based

Single-cycle

Efficient for deep CAMs

Single match only → Cannot be cascaded → RAM depth is exponential to pattern width → Inefficient for wide patterns

Indirectly-Indexed 2D (II2D) BCAM (1) Cascadable Wide and Deep BCAM

PROBLEM: is it possible to regenerate matches for all addresses?

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Key observation	
Transposed RAM is a sparse matrix	*n* columns (set of addresses) accommodates *n* matches (1's) at most!

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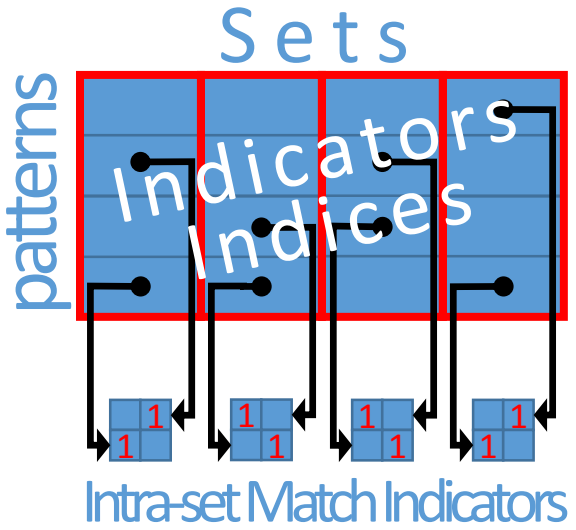

Key idea: use indirect indices to point to intra-set matches

↓

Cascadable

↓

Scalable (linear growth)

↓

Supports wider patterns

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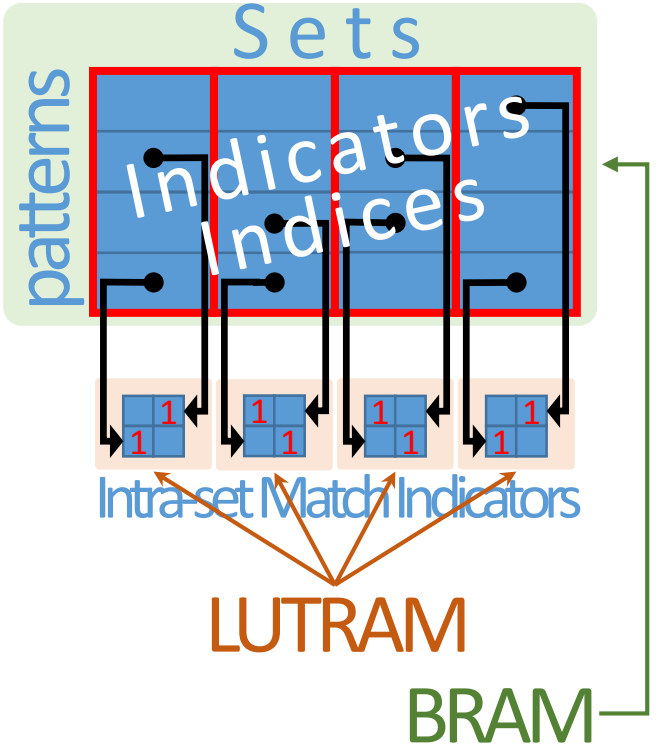

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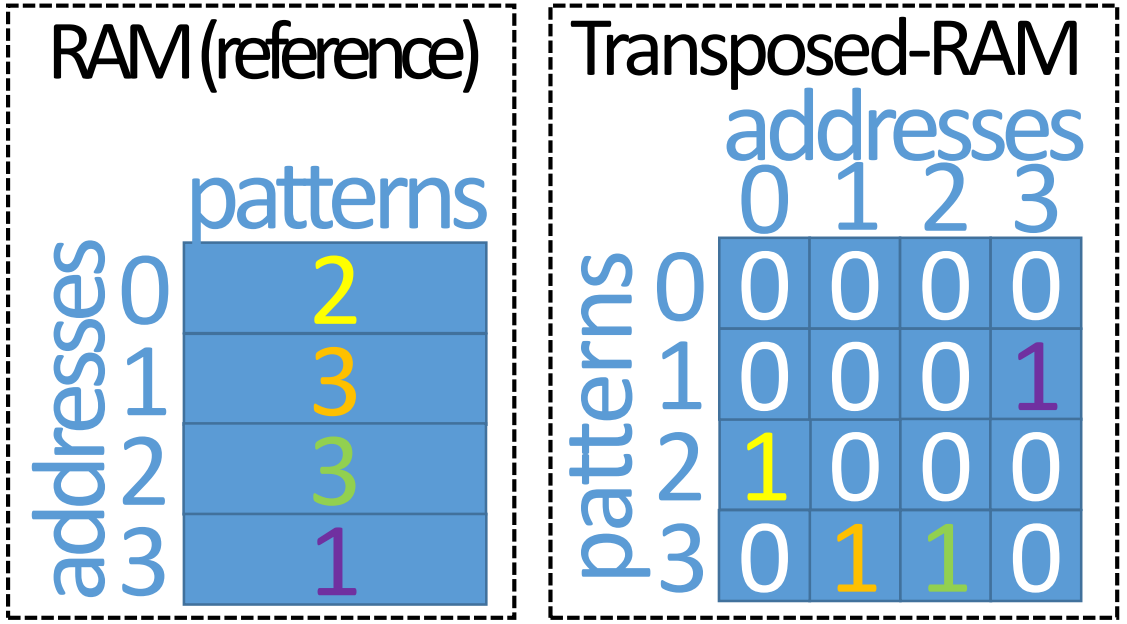

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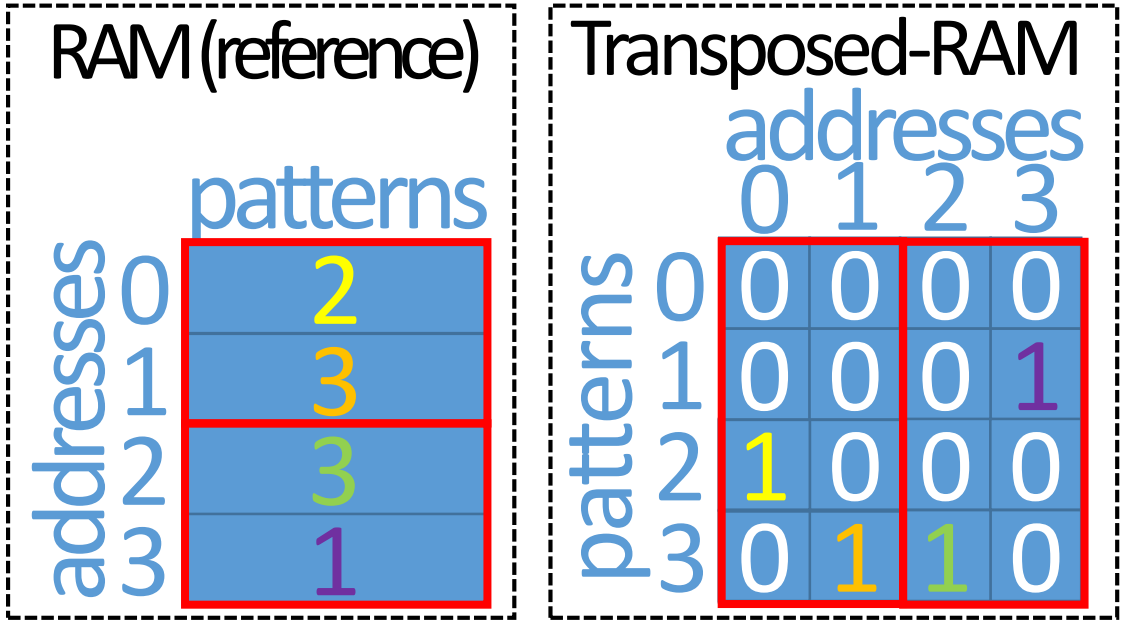
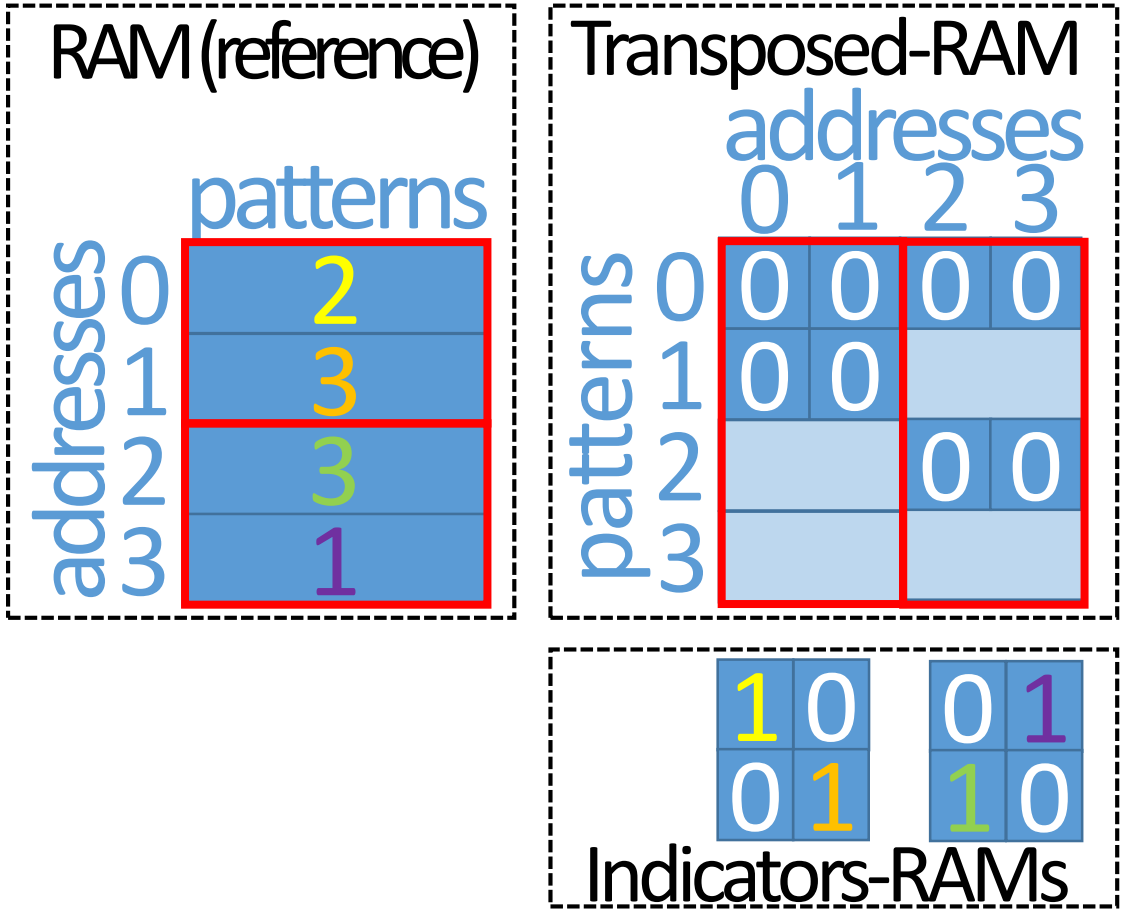


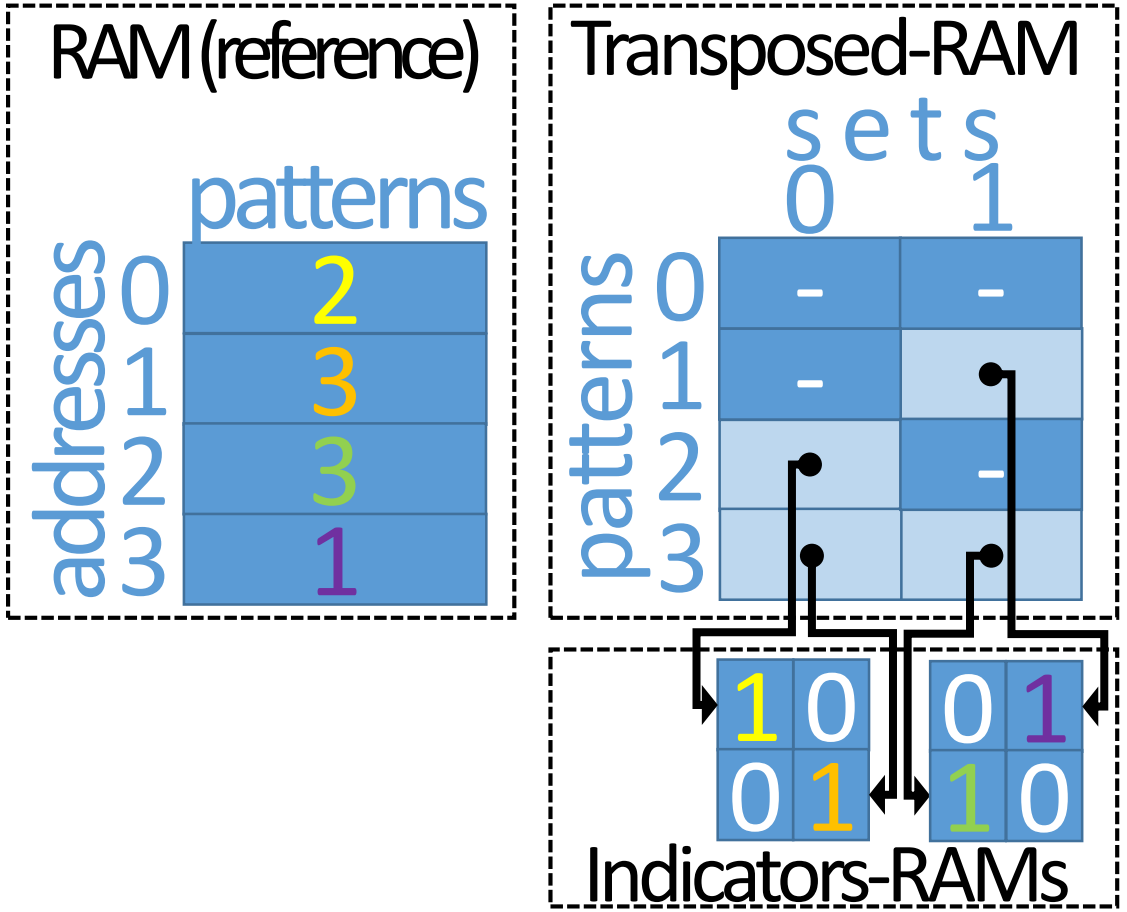
Indirectly-Indexed 2D (II2D) BCAM (2) Example

- Divide address space into sets
- Store sets with a match in Indicators-RAM



Indirectly-Indexed 2D (II2D) BCAM (2) Example

- Divide address space into sets
- Store sets with a match in Indicators-RAM
- Transposed-RAM stores indices to all matches in set



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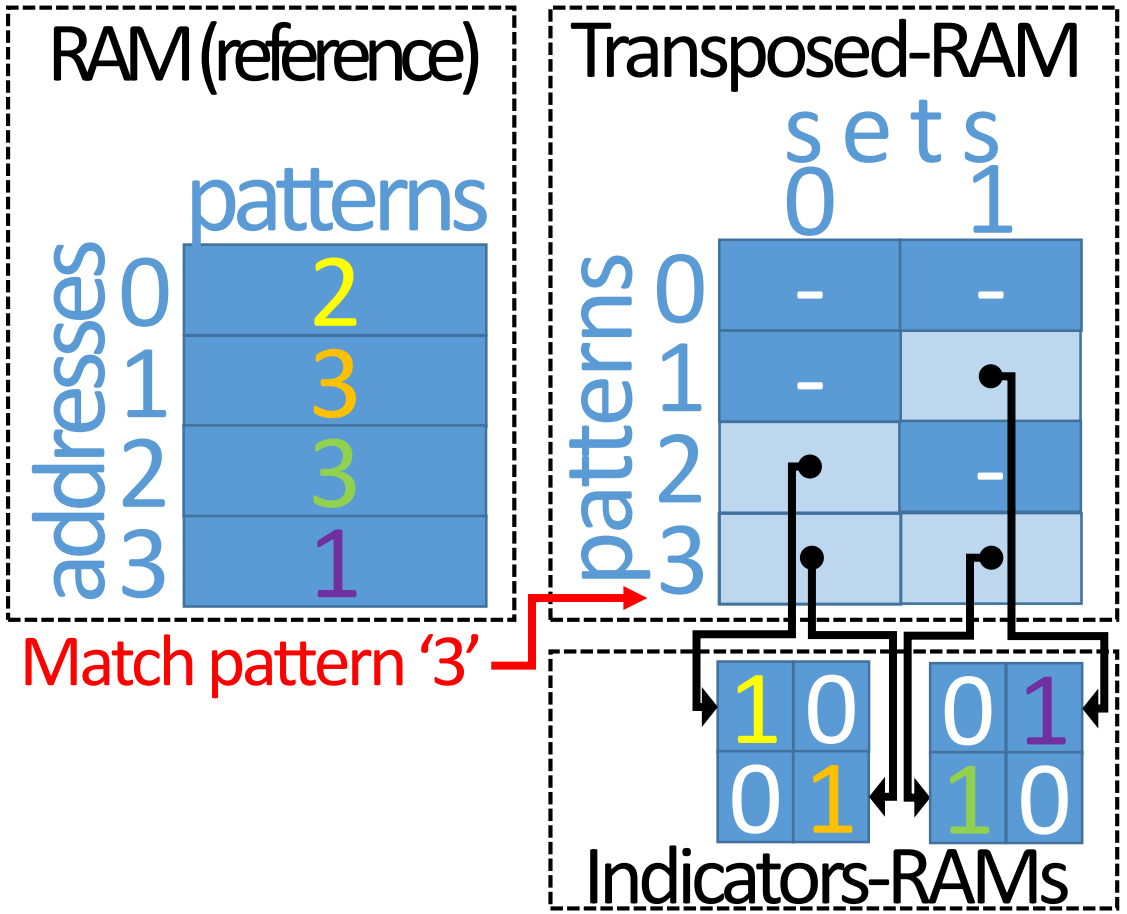

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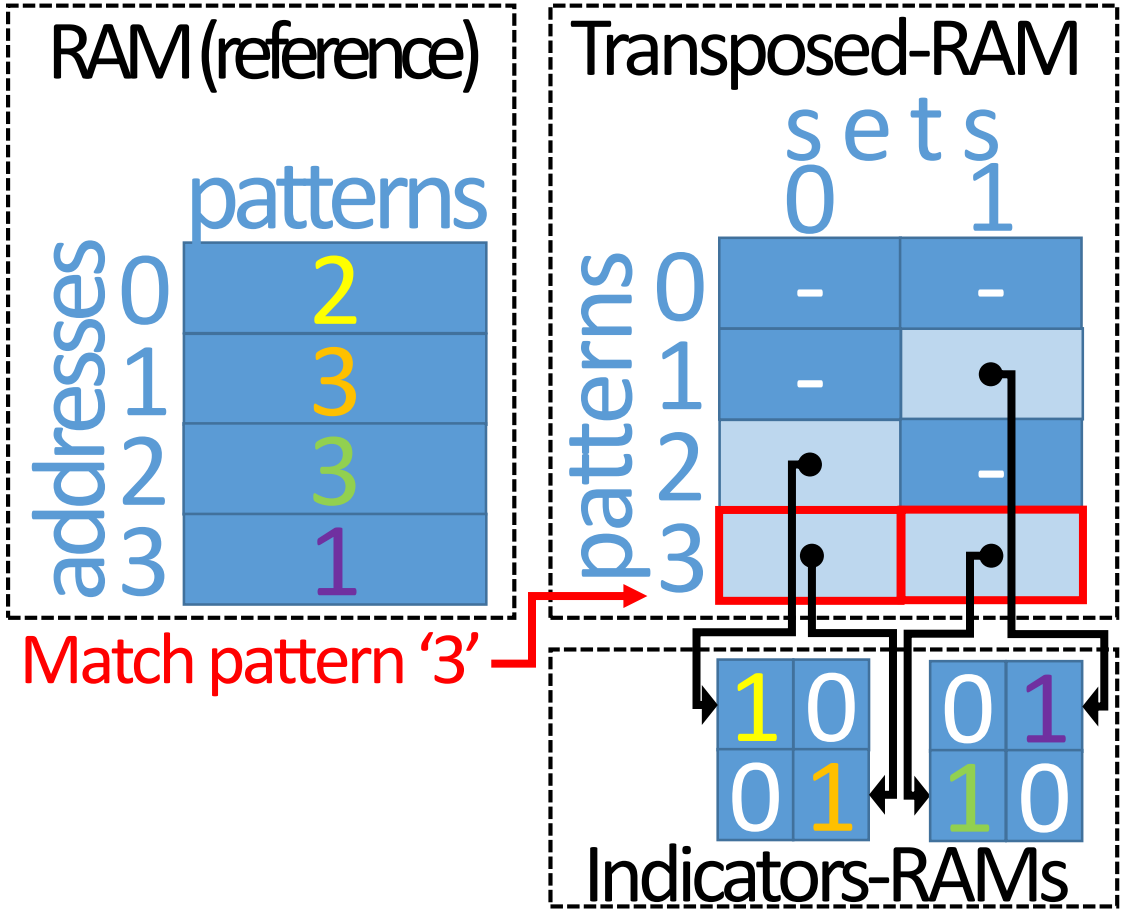

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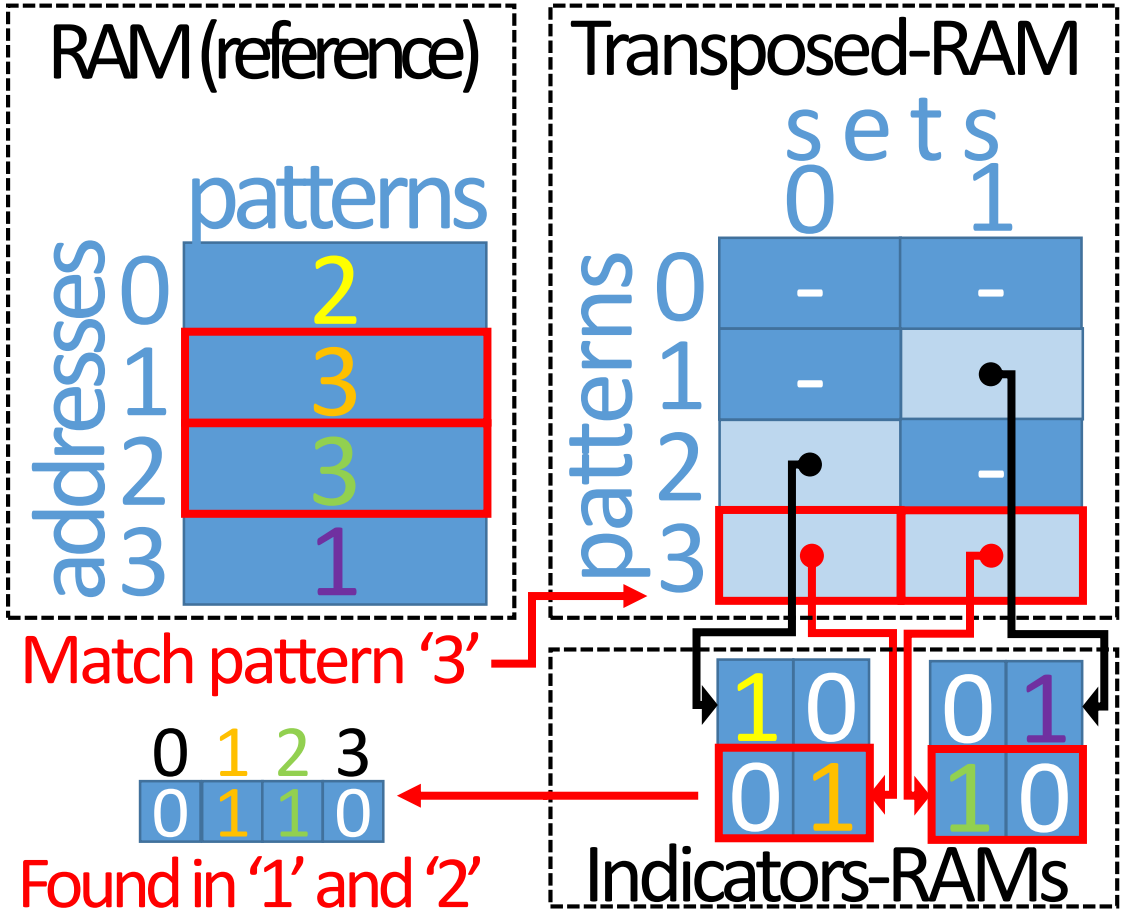
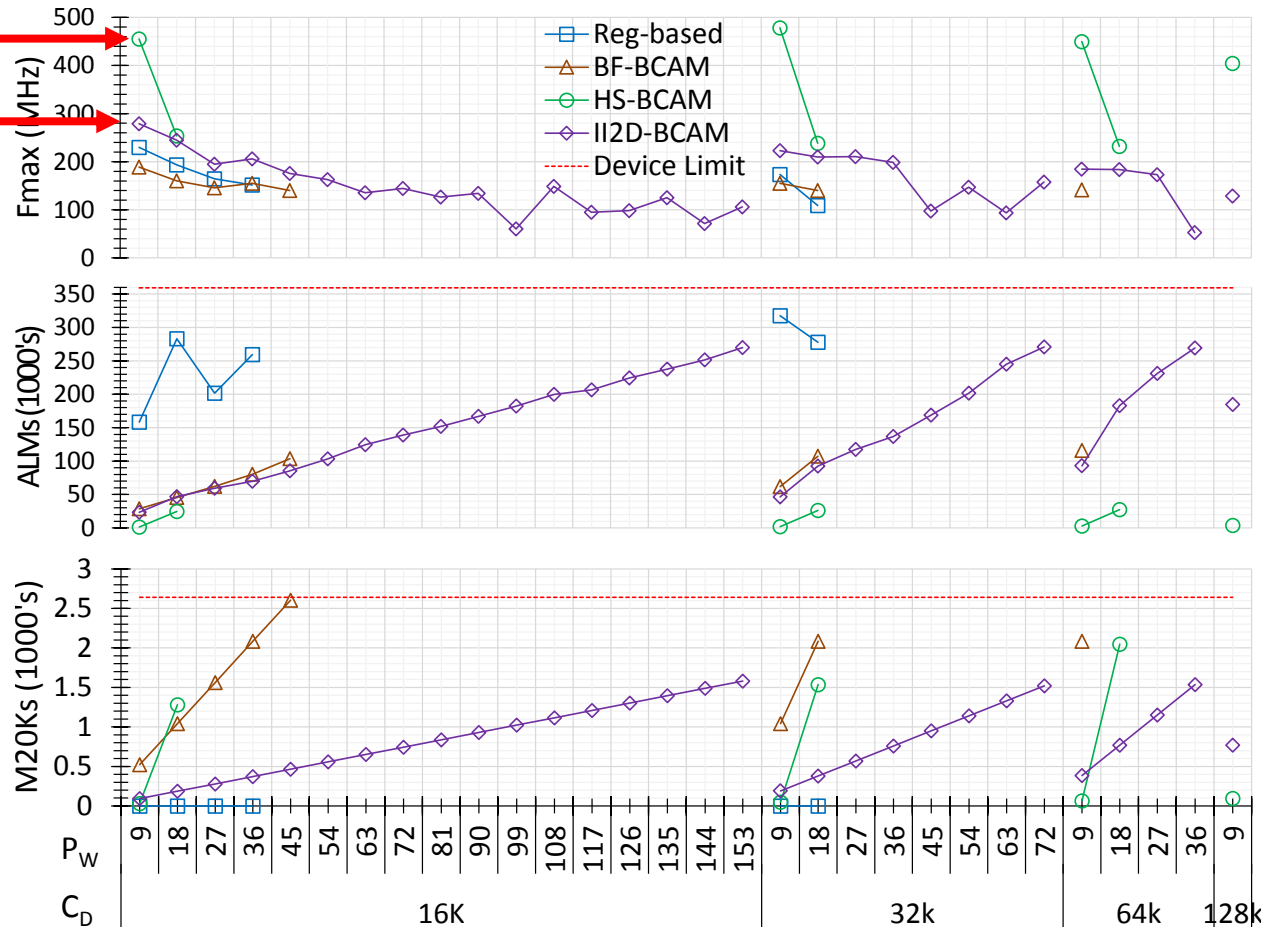
  - Find indices of all matching sets in Transposed-RAM
  - Read Indicators-RAM using indices from Transposed-RAM



Indirectly-Indexed 2D (II2D) BCAM (3) Area and Performance

Except for very a narrow HS,
II2D exhibits higher Fmax



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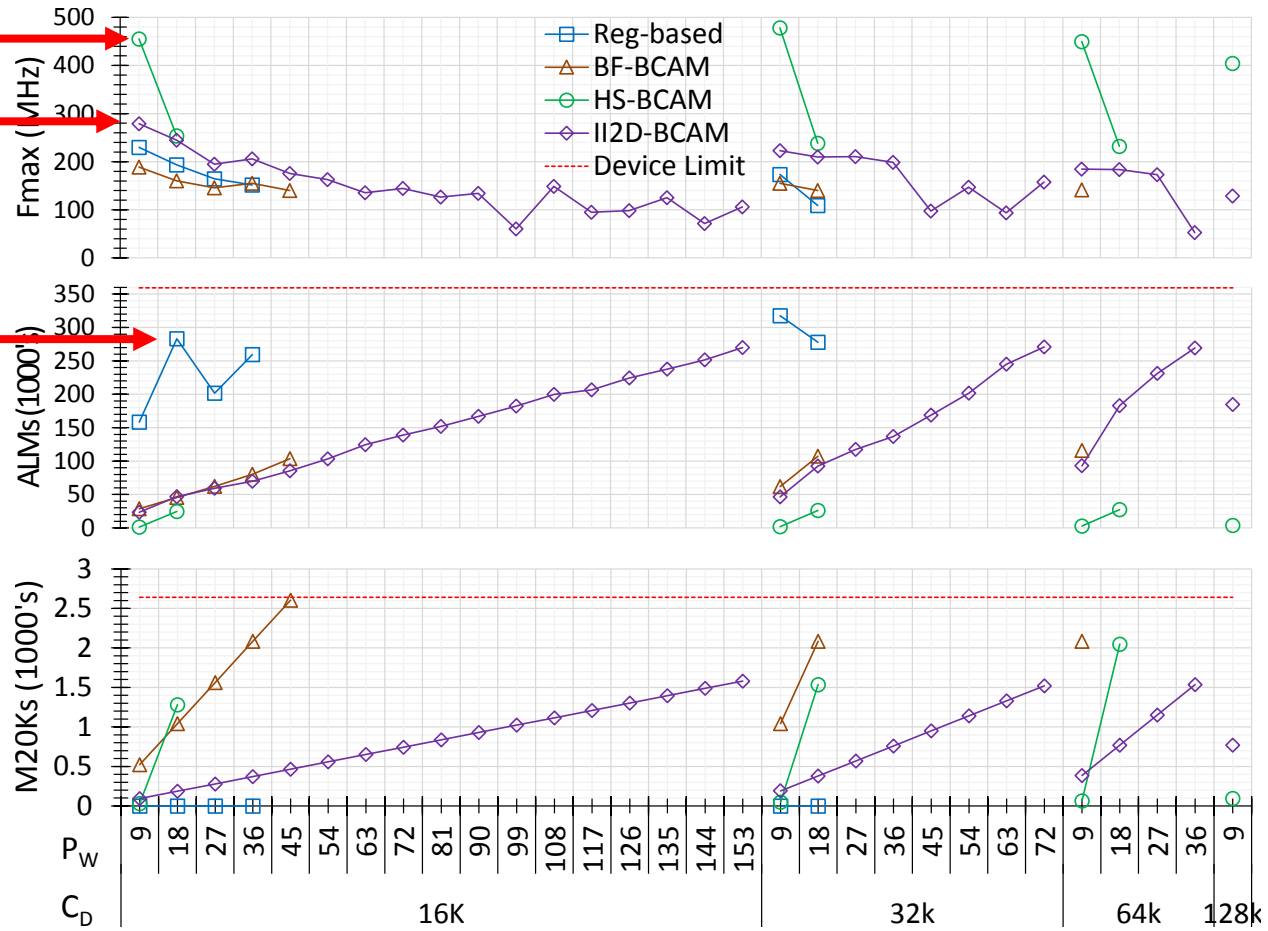

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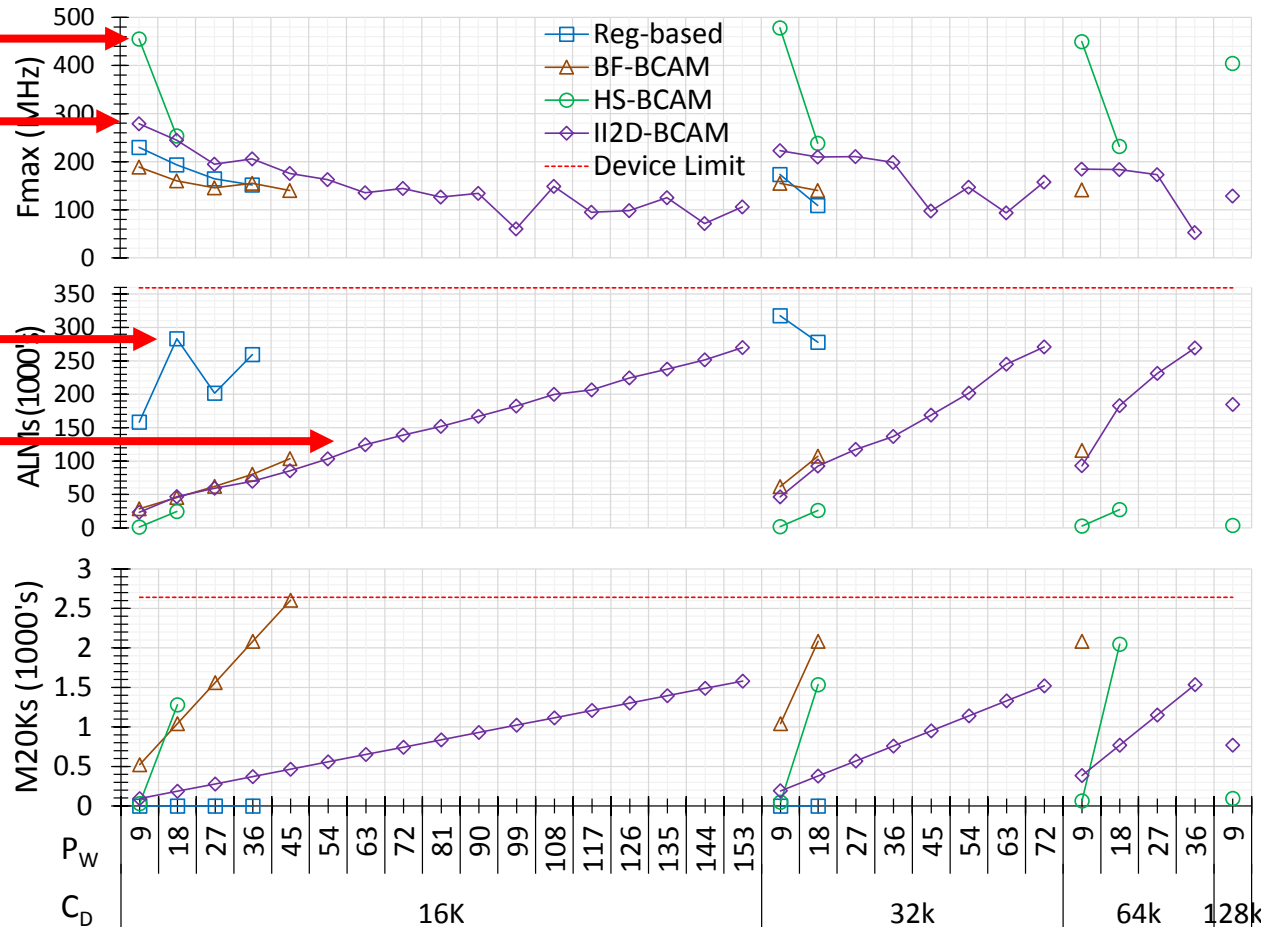

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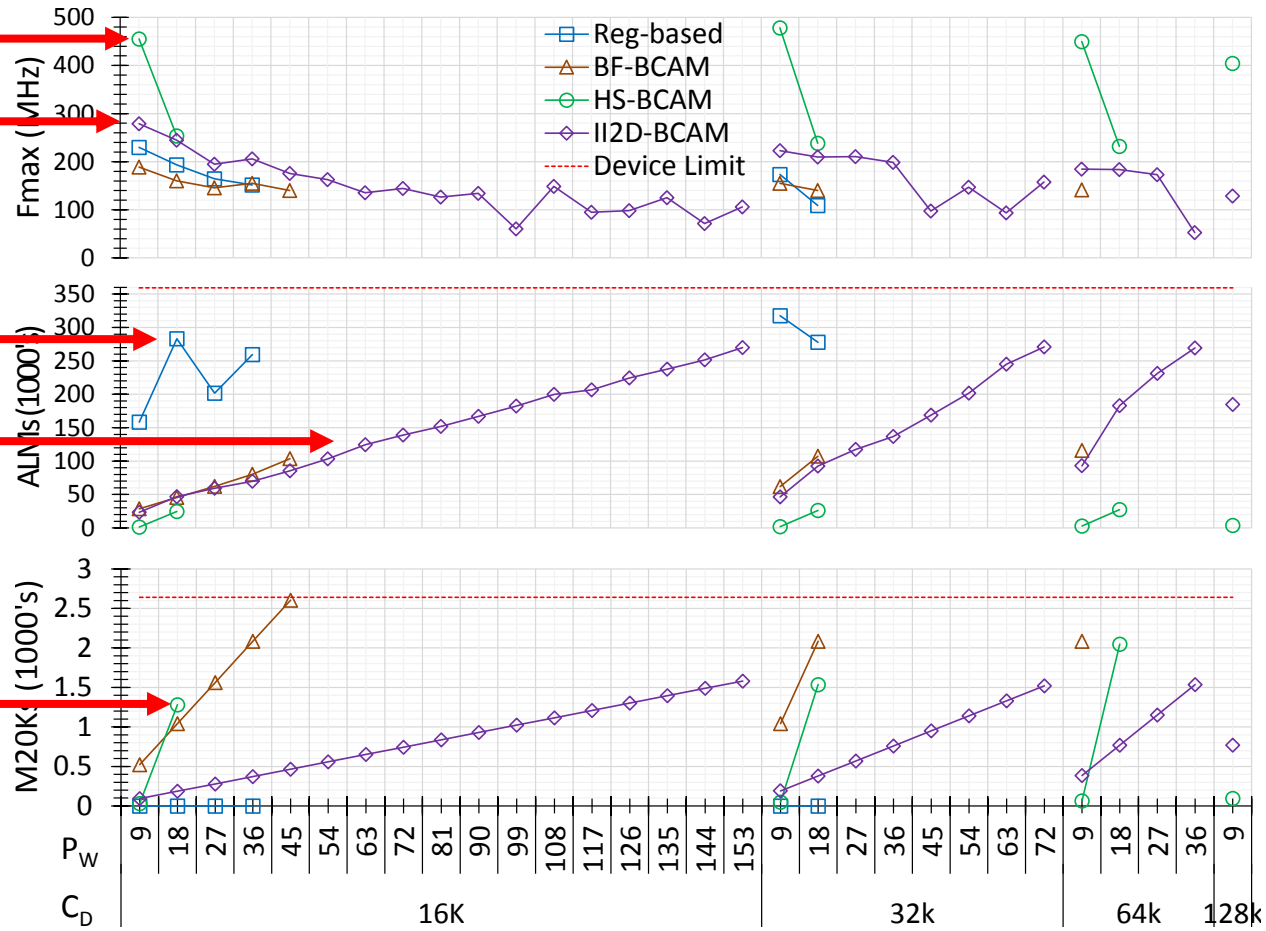

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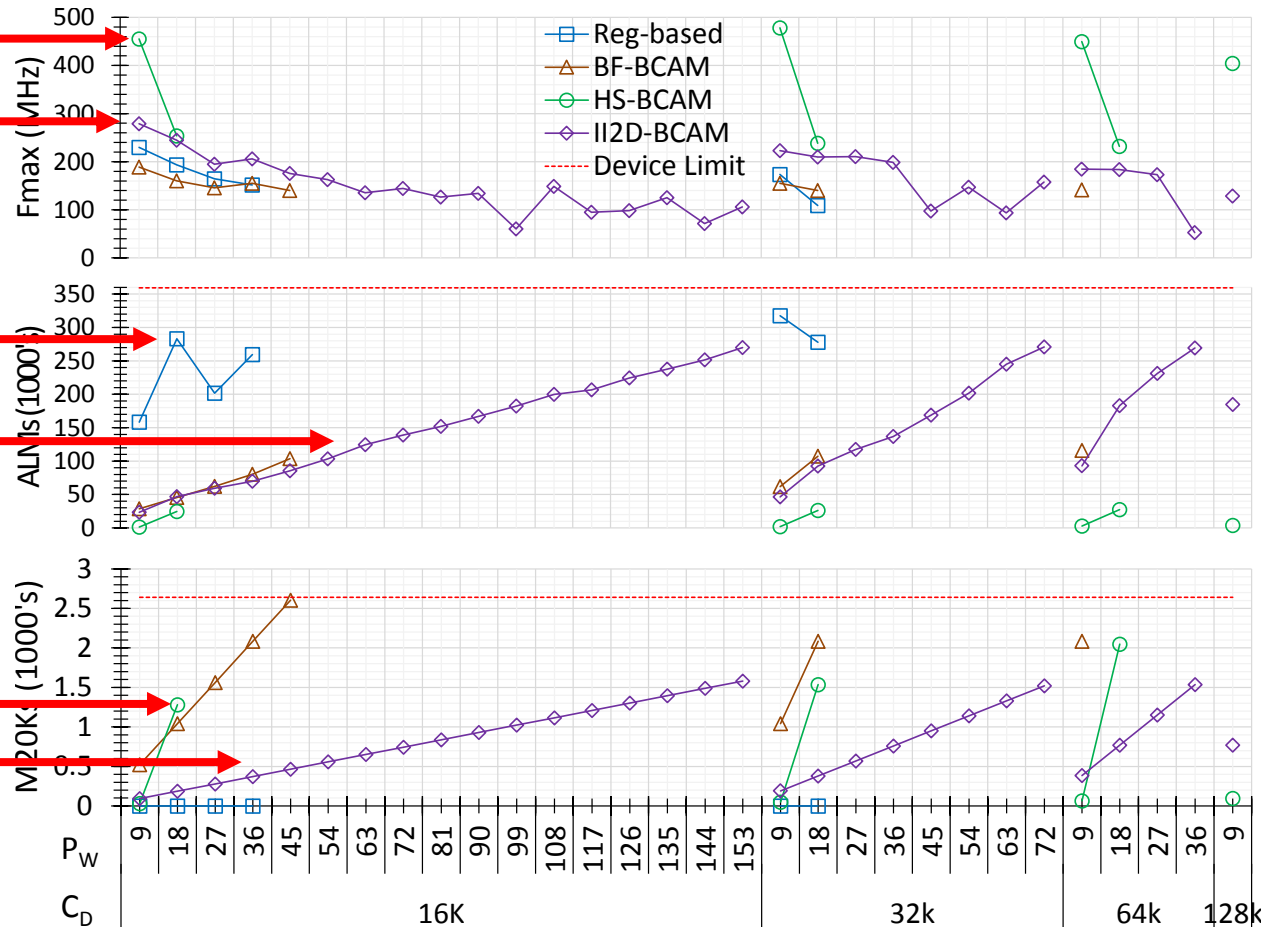

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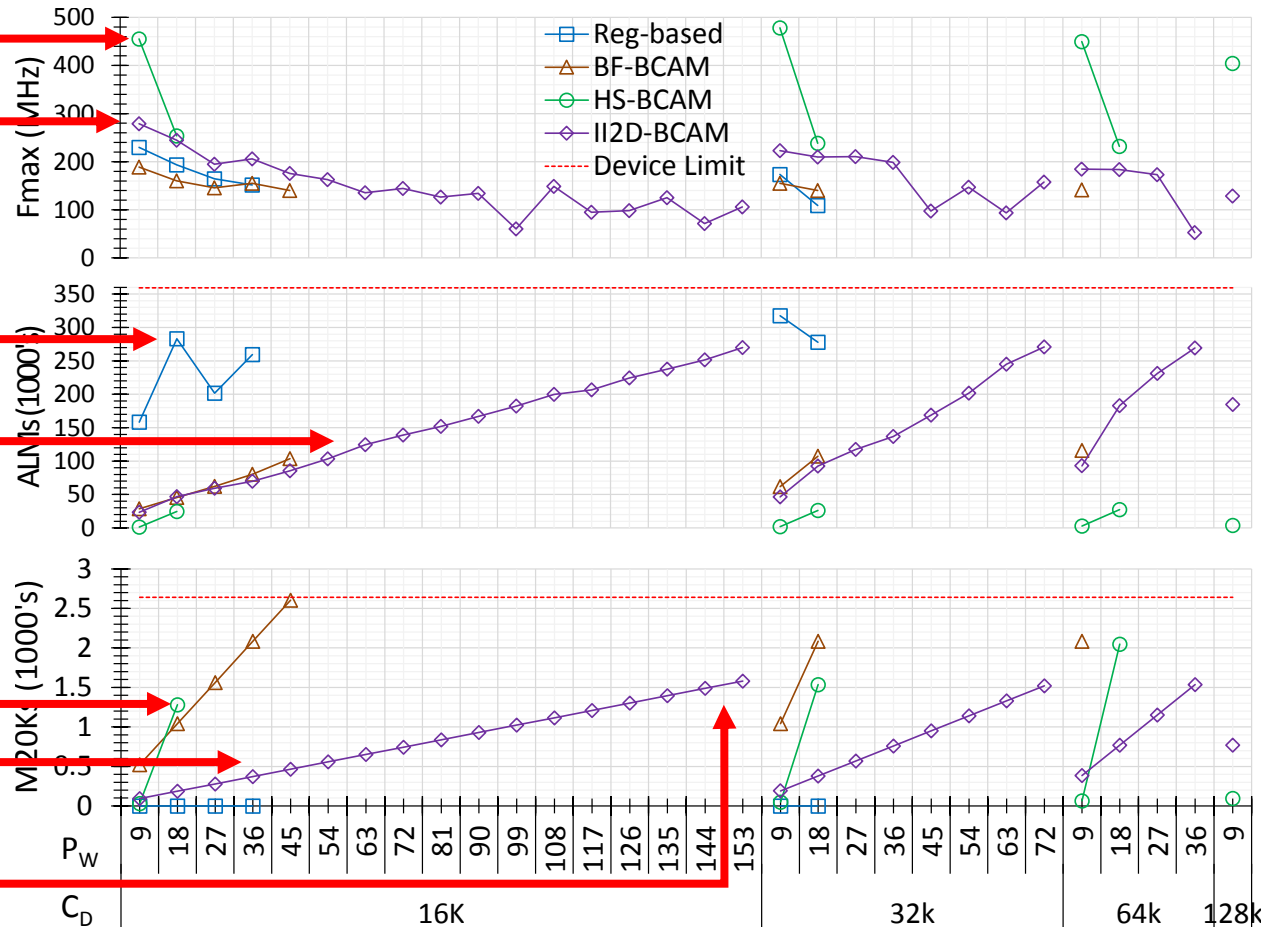


Open Source

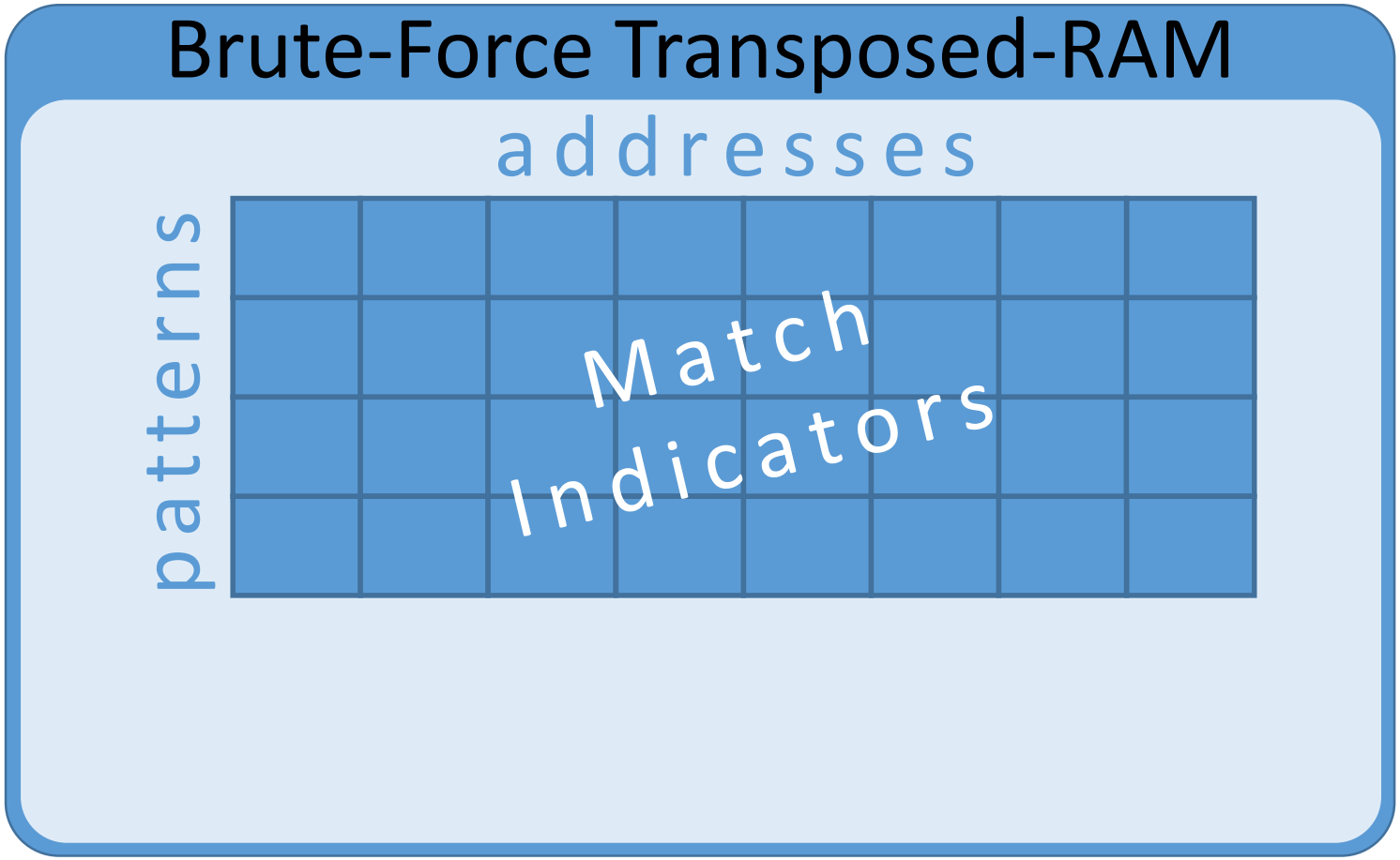
http://ece.ubc.ca/~lemieux/downloads/

Modular and parametric Verilog files

Run-in-batch simulation and synthesis manager

Conclusions

- BRAM-based ✓
- Single-cycle ✓
- Cascadable ✓
- Scalable ✓
- Deep ✗
- Wide ✓



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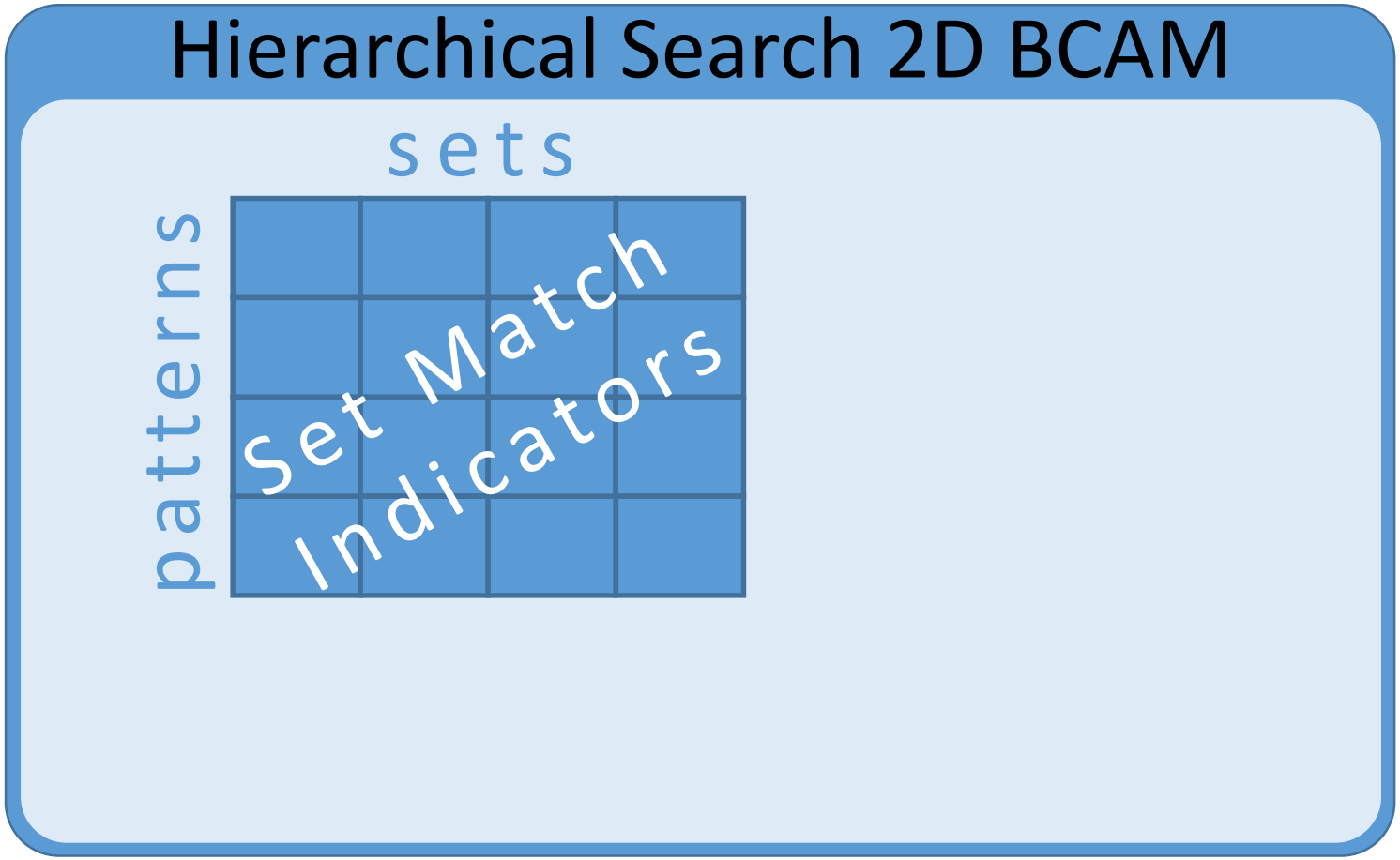

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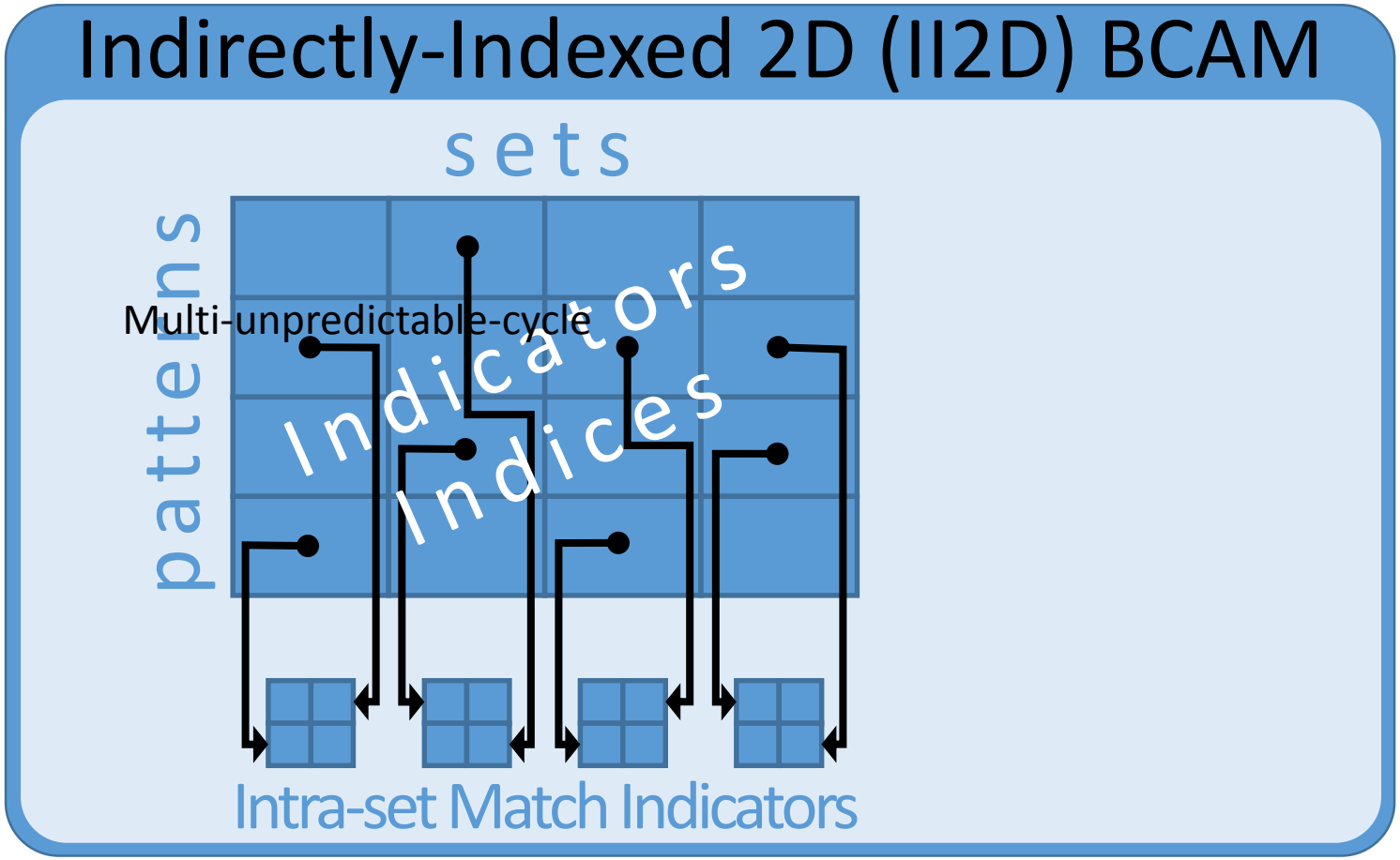

Thank You!

Backup Slides

Conclusions