Automatic High-Level Hardware Checkpoint Selection for Reconfigurable Systems

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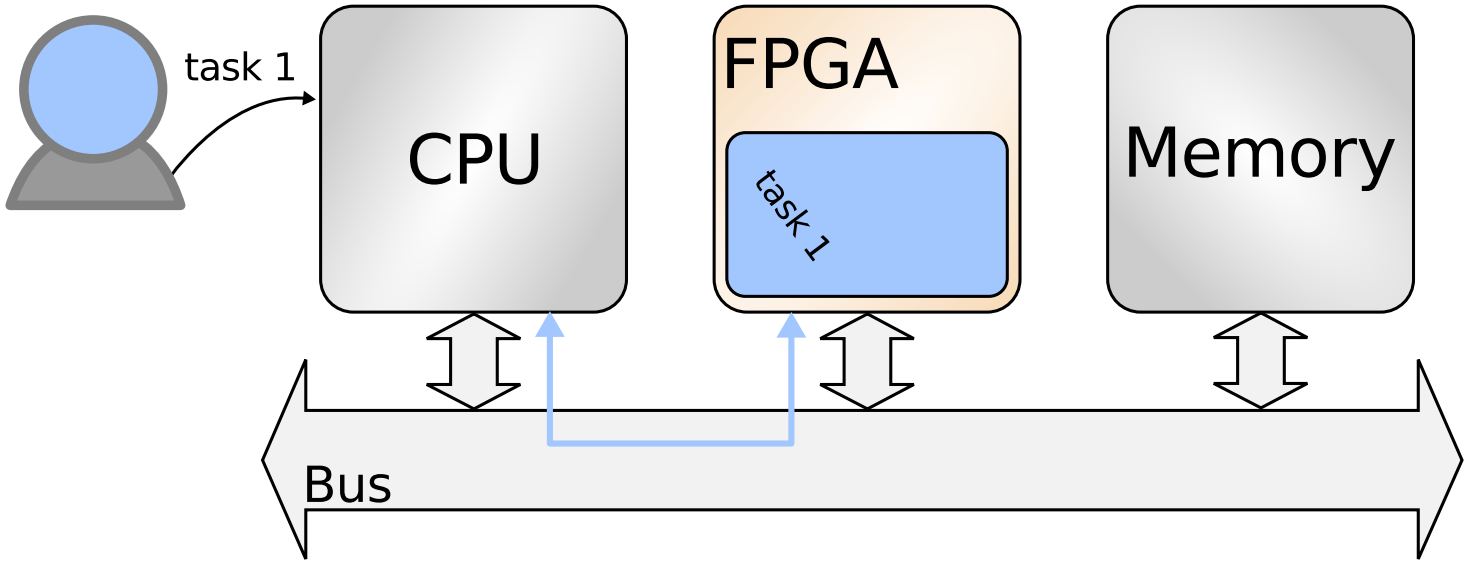
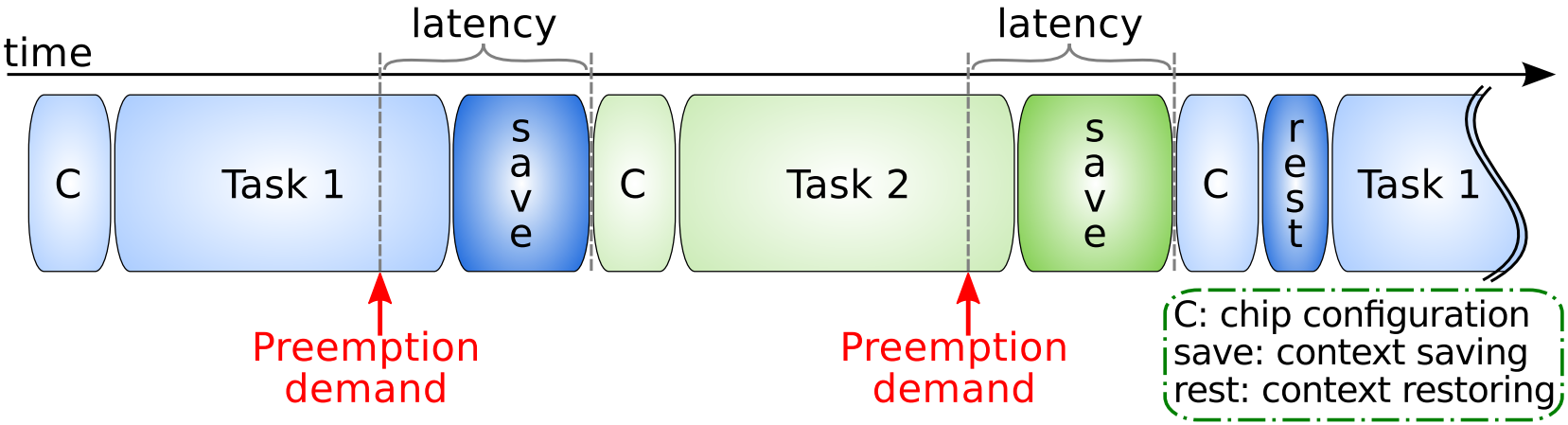
Hardware context switch





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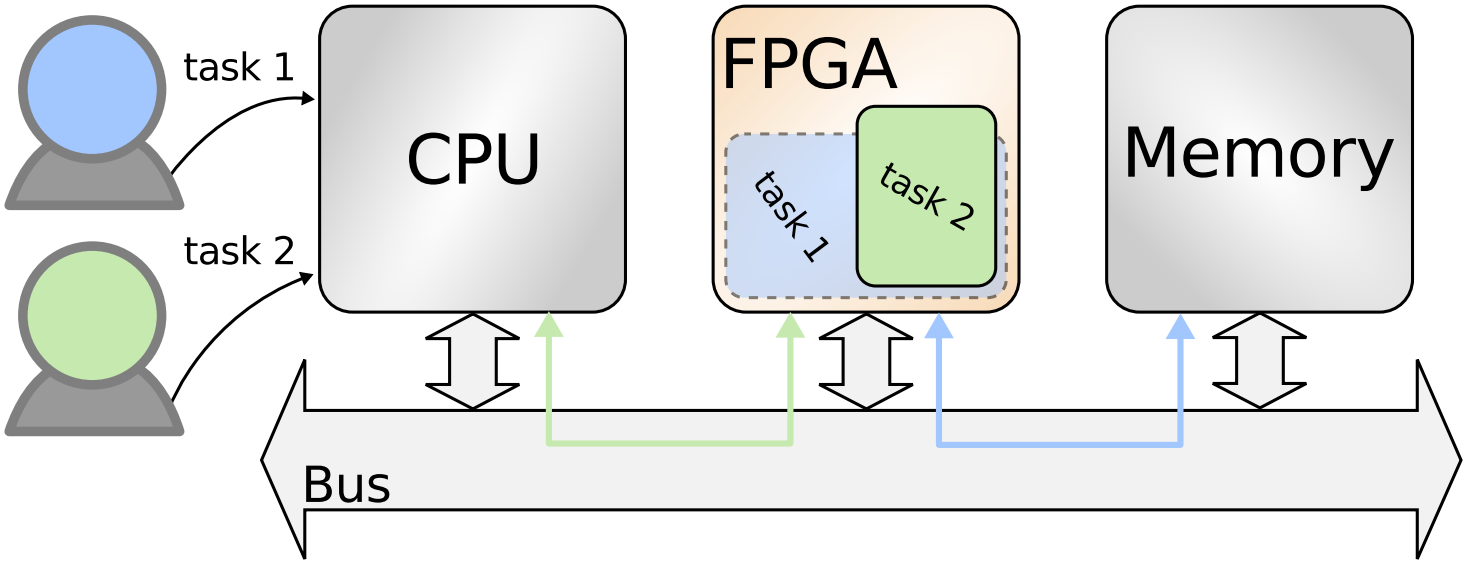

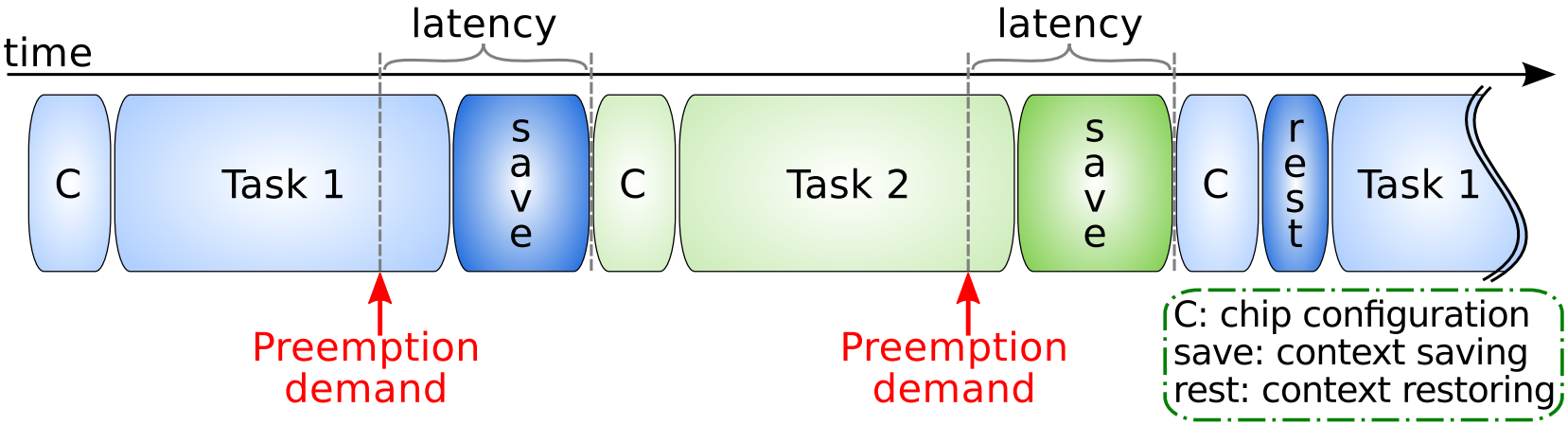

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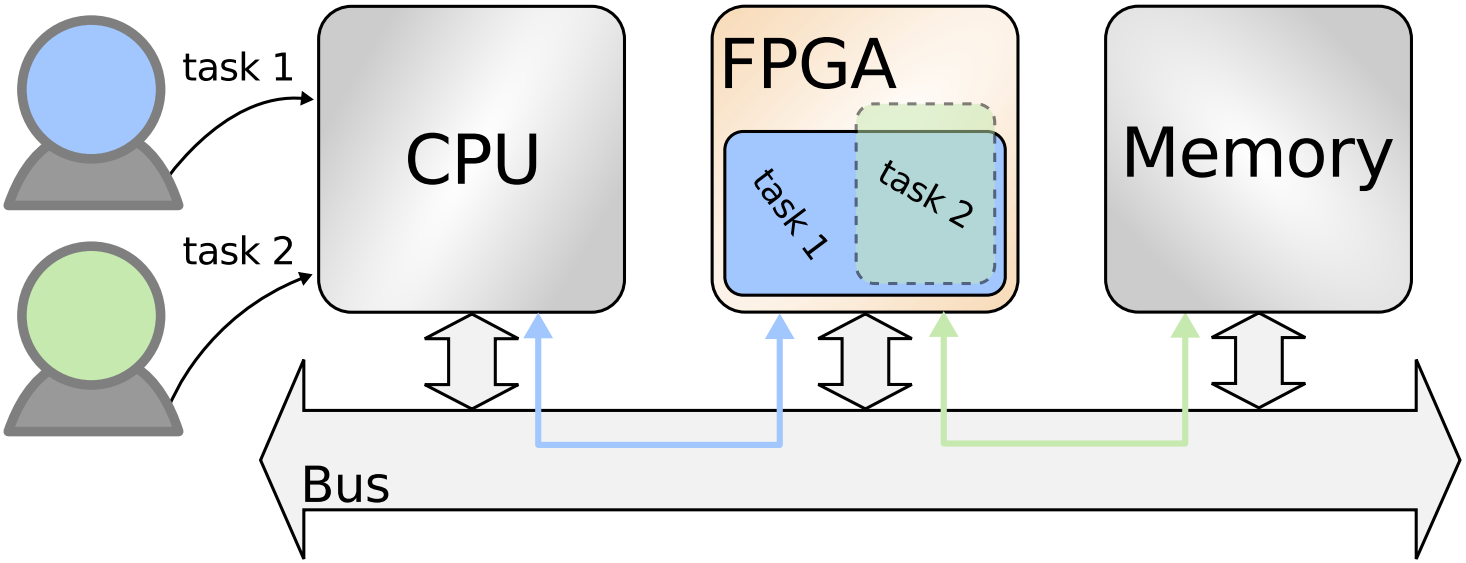
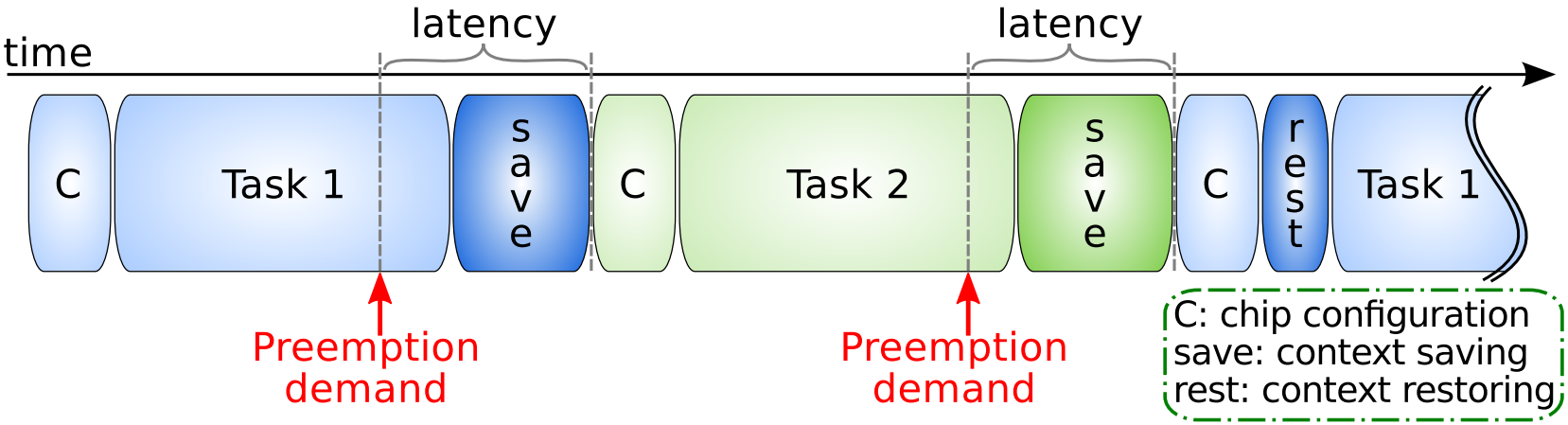
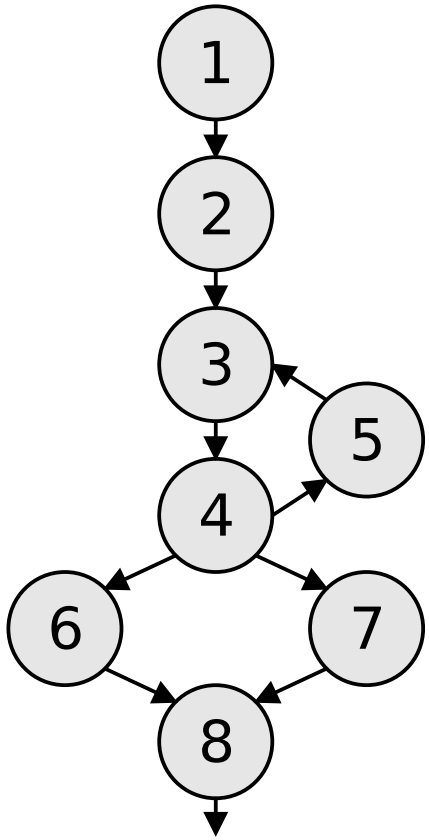




Contributions

Algorithm with 2 inputs:

- FSM of the HW task
- Latency



Contributions

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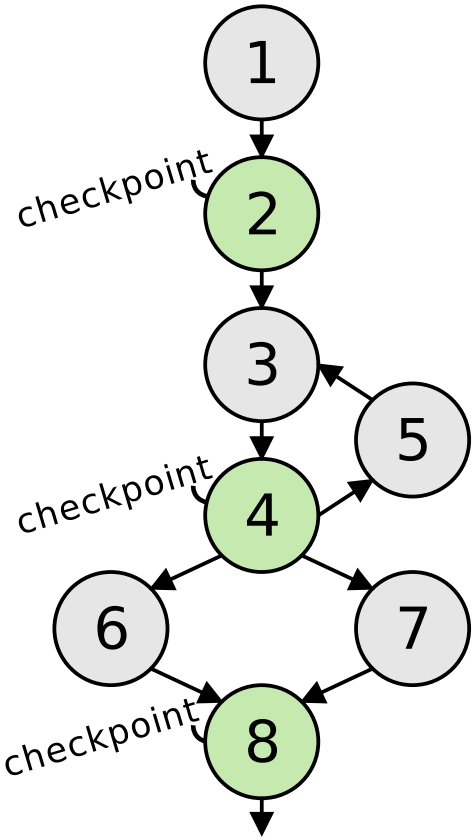
- FSM of the HW task
- Latency

$\Rightarrow$ set of checkpoints

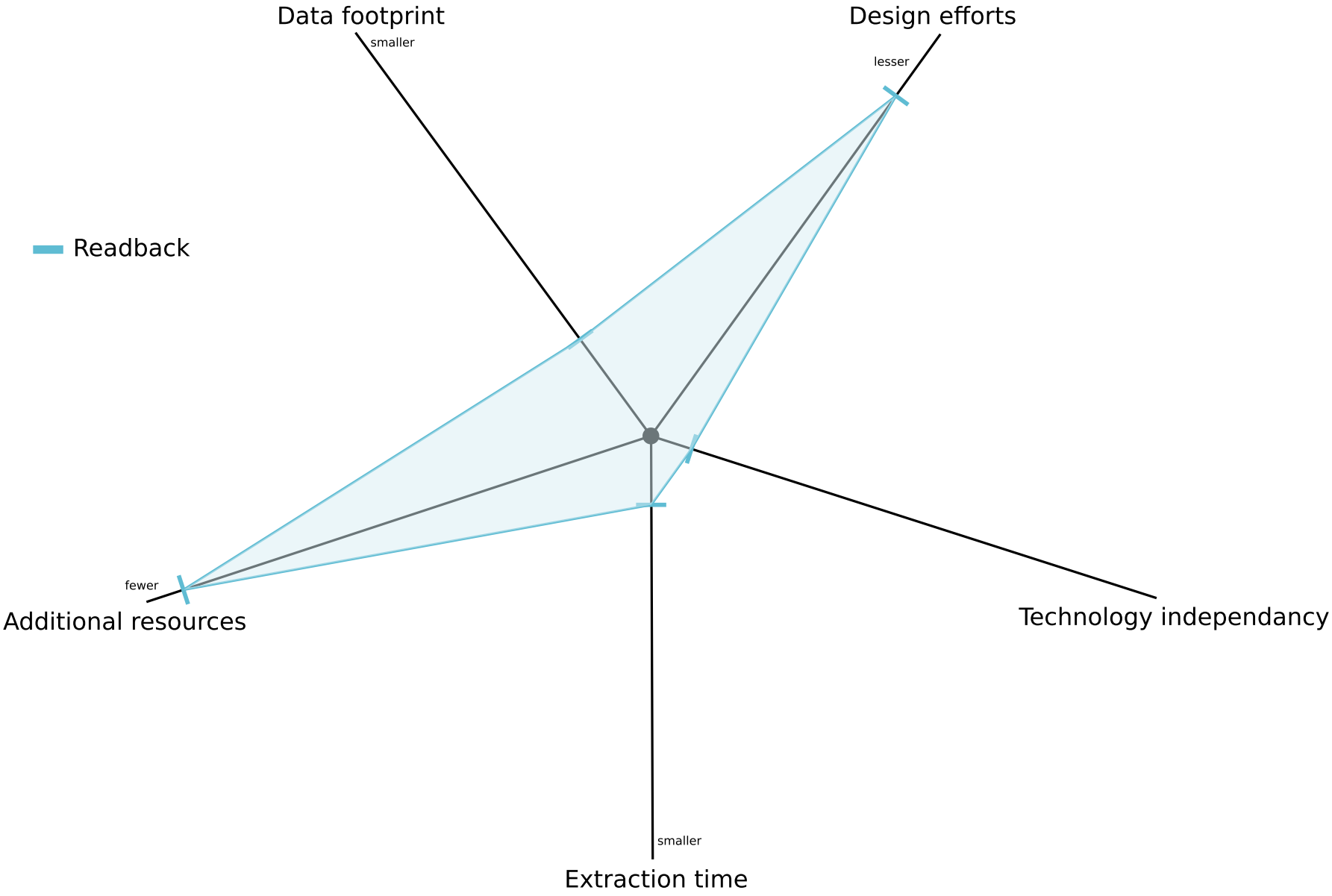
Circuit produced:

- Minimized area overhead
- Reduced memory footprint
- Respect preemption latency

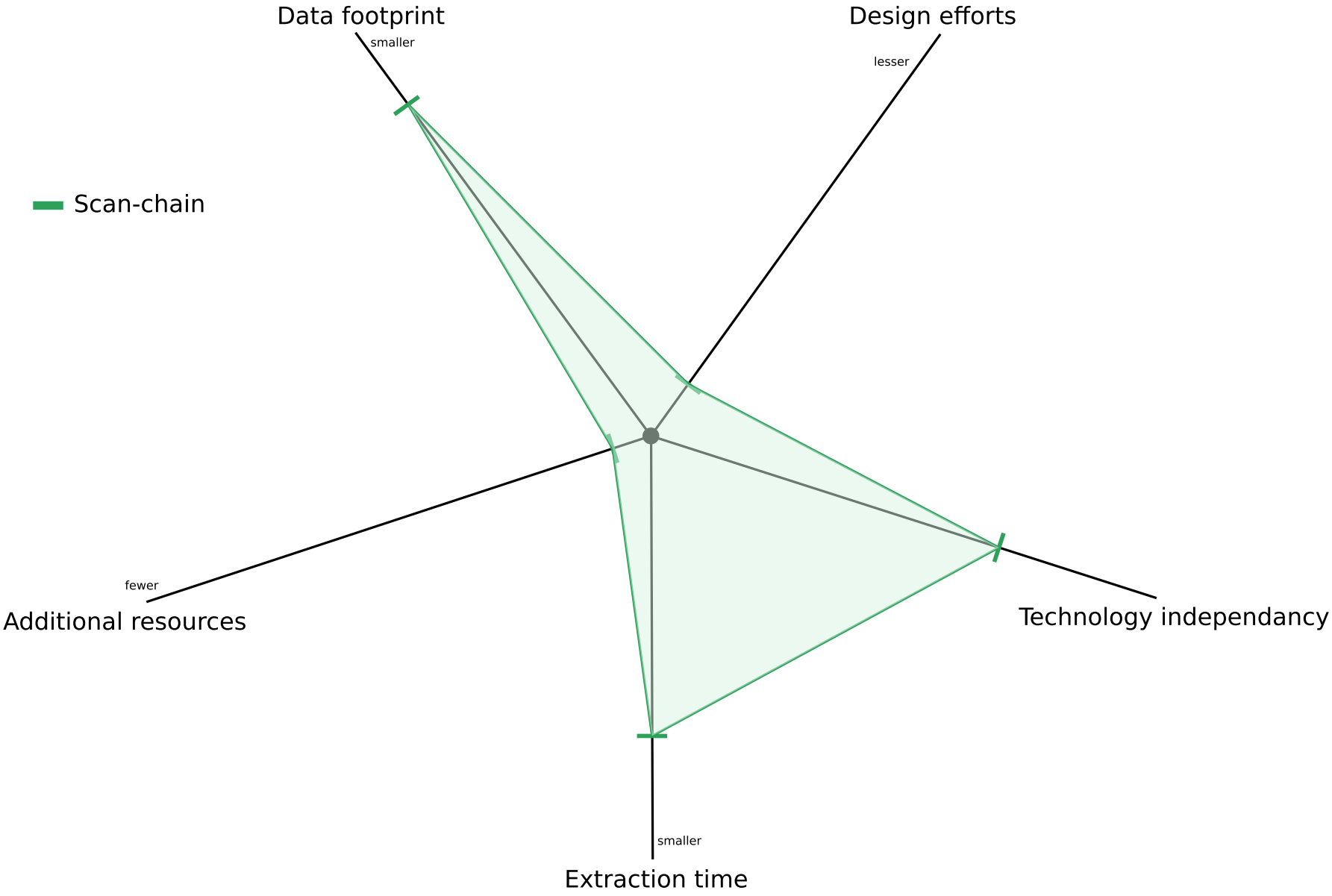
Algorithm implemented in an HLS tool



Comparison


Data footprint
smaller
Design efforts
lesser
Readback
fewer
Additional resources
Technology independancy
smaller
Extraction time

Comparison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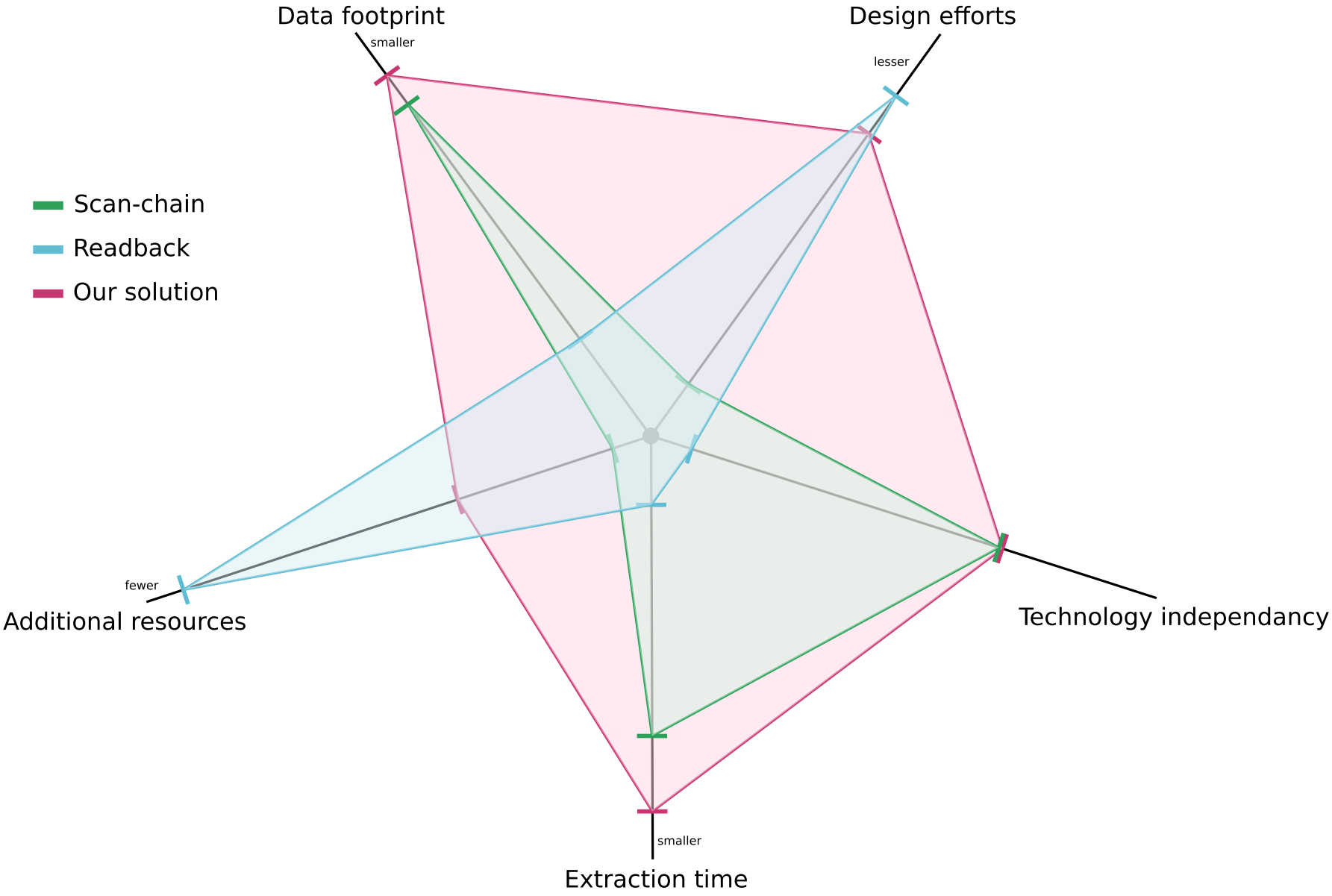
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Our solution
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During poster session

Further presentation of contributions:

- results !
  85% less memory elements to save
  52% HW overhead reduction
- more details about the method and implementation
- come and see our open source HLS tool AUGH and its plugin CP3