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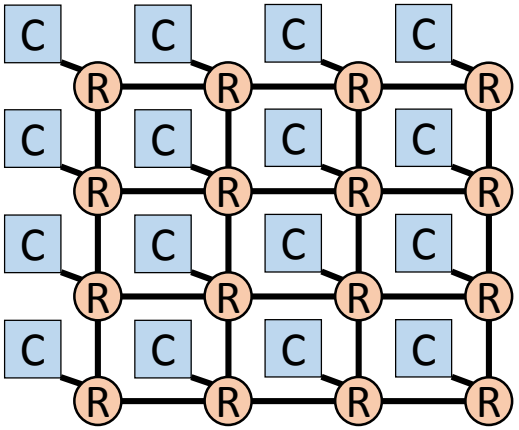
Enabling Fast and Accurate Emulation of Large-scale Network on Chip Architectures on a Single FPGA

Thiem Van Chu[1)], Shimpei Sato[2)], and Kenji Kise[1)]

[1)]Tokyo Institute of Technology

[2)]Japan Advanced Institute of Science and Technology

Introduction



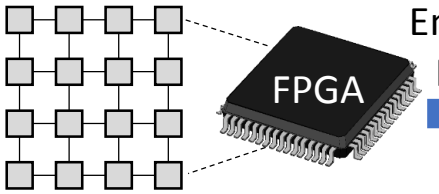
C Core
R Router

Network on Chip (NoC)
On-chip communication backbone

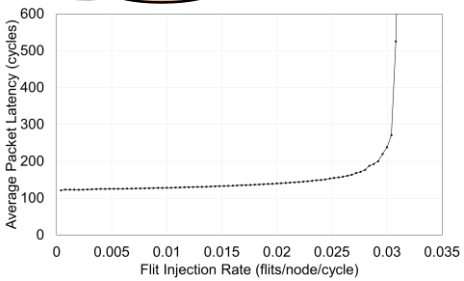
- Software-based simulators
  - E.g. Booksim [Jiang+, ISPASS'13]
  - Flexible and easy to debug
  - Slow

- FPGA-based emulation

Very fast



Emulation Results



Single FPGA →
- Limited resources
- Large FPGA → ~100 routers

Multiple FPGAs
Off-chip memory
[Nejad+, DATE'11]
[Wolkotte+, NOCS'07] →
- Complex
- Off-chip communication

Our Approach

- Time-multiplexing: emulate the entire network using several physical nodes
- Decoupling time counters: eliminate the memory constraint in open-loop simulations

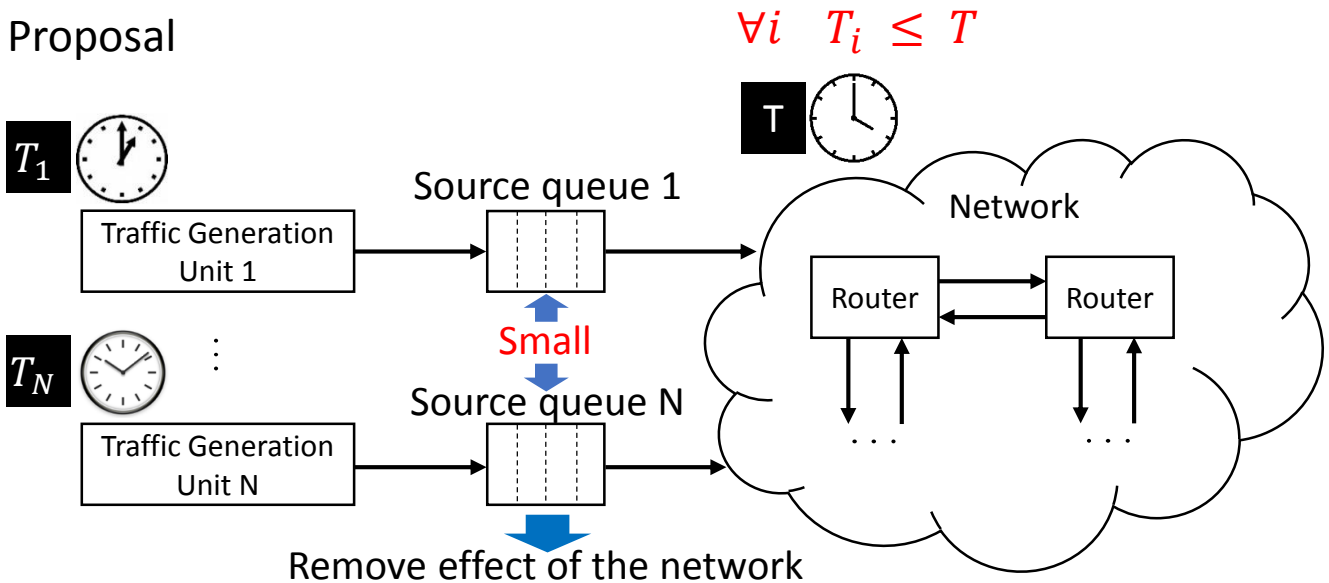
Fast and accurate emulation of large NoC designs on a single FPGA

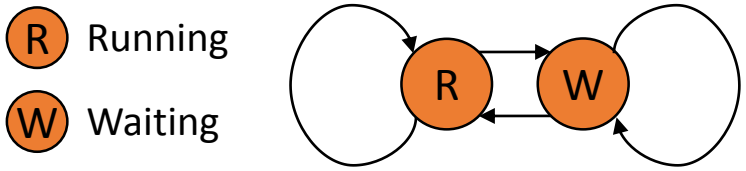
Key ideas

Time-multiplexing

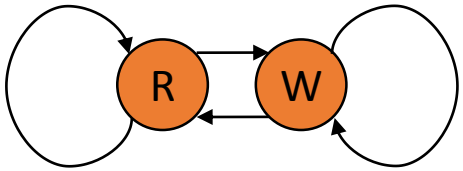
Decoupling time counters

- Convention
  - $\forall i \quad T_i = T$
  - Needs very large source queues
- Proposal
  - $\forall i \quad T_i \leq T$
  - Small source queues are OK





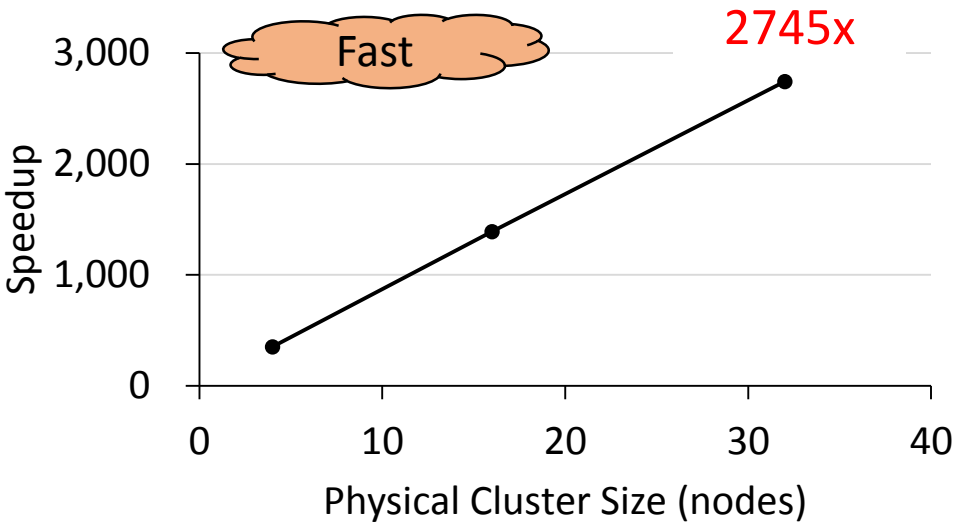
State transition of each traffic generation unit

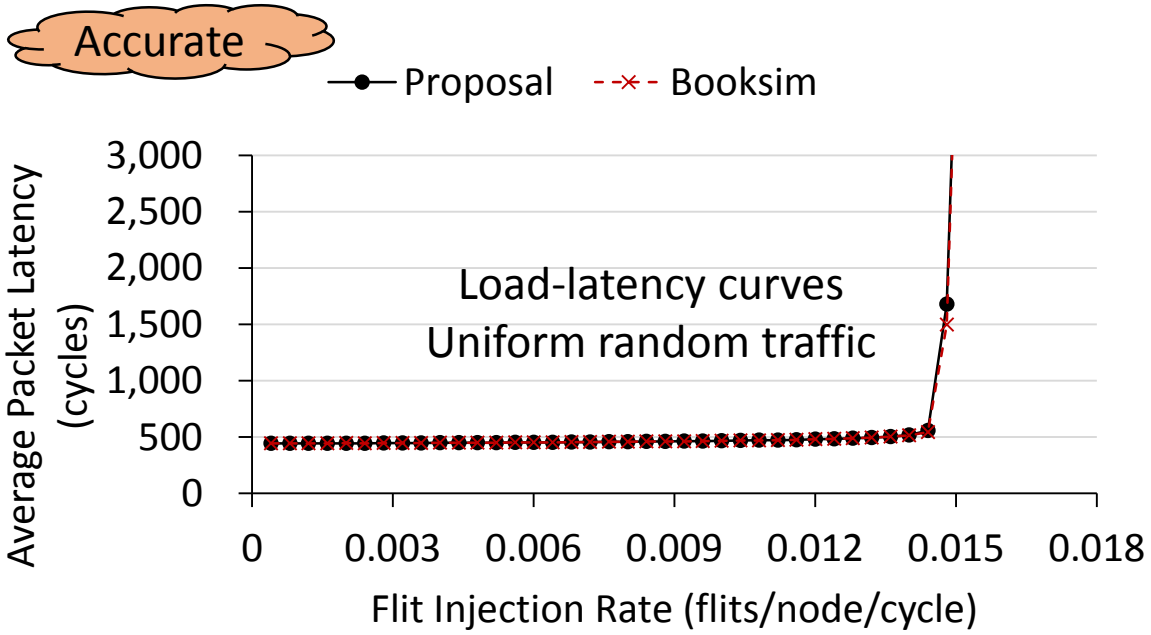


State transition of the network

Evaluation

- 128x128 mesh network (16,384 nodes)
- Conventional 5-stage pipelined router architecture (2VCs/port)





High end PC
core i7 4770 CPU
32GB RAM

Booksim: > 162 hours

Proposal: < 3 minutes

Virtex-7 FPGA

Conclusion

- We propose two methods to enable fast and accurate emulation of large-scale NoC architectures on a single FPGA
- 2745x simulation speedup over Booksim is achieved when emulating an 128x128 NoC design with the state-of-the-art 5-stage pipelined router architecture