Technology Scaling in FPGAs

Trends in Applications and Architectures

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Motivation

- First commercial FPGA was released in 1985
- FCCM has more than 20 years of history
- Can we learn something about progress based on past designs?

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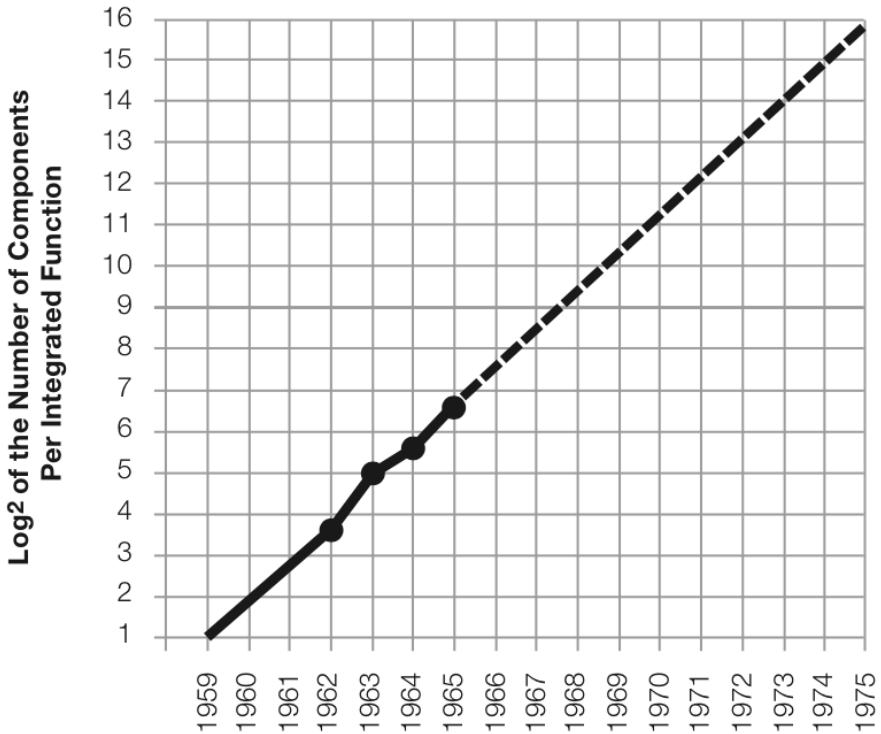
Aims

- Develop models of area and speed across generations of FPGA devices
- See how device trends compare with those expected by Moore's Law and Dennard's Law
- Compare performance of devices to designs published at FCCM
  - Odd years (total of 284 designs)
- Develop model which can be used for extrapolation
  - How does this model compare using vendor cores to scale technologies?
  - How does it perform looking forward?

Moore's Law

- Gordon Moore in 1965 predicted number of transistors in an IC will double ≈ two years



Electronics, v 38, n 8, April 19, 1965.

Moore's Law

- He made the bold claim that 65,000 components could fit on an IC by 1975 (at the time they had 50)!
- Cartoon is from the same paper

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Dennard's Law

› Dennard in 1974: as transistor feature size (κ or commonly λ) decreases, power stays proportional to area

Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, L, W	$1/\kappa$
Doping concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $\epsilon A/t$	$1/\kappa$
Delay time/circuit VC/I	$1/\kappa$
Power dissipation/circuit VI	$1/\kappa^2$
Power density VI/A	1

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Normalising Resource Usage

How do we compare designs over process technologies:

- 4-LUTs and 6-LUTs?
  - Altera ALM = 2.5 4-LUTs
  - Xilinx 6-LUT = 1.4 4-LUTs

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Normalising Resource Usage

How do we compare designs over process technologies:

- Multipliers DSP/blocks
  - Altera DSP blocks counted as number of 18x18 multipliers
  - All Xilinx multipliers (whether 18x18 or 25x18) considered an 18x18 multiplier

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  - Just using number of kilobits

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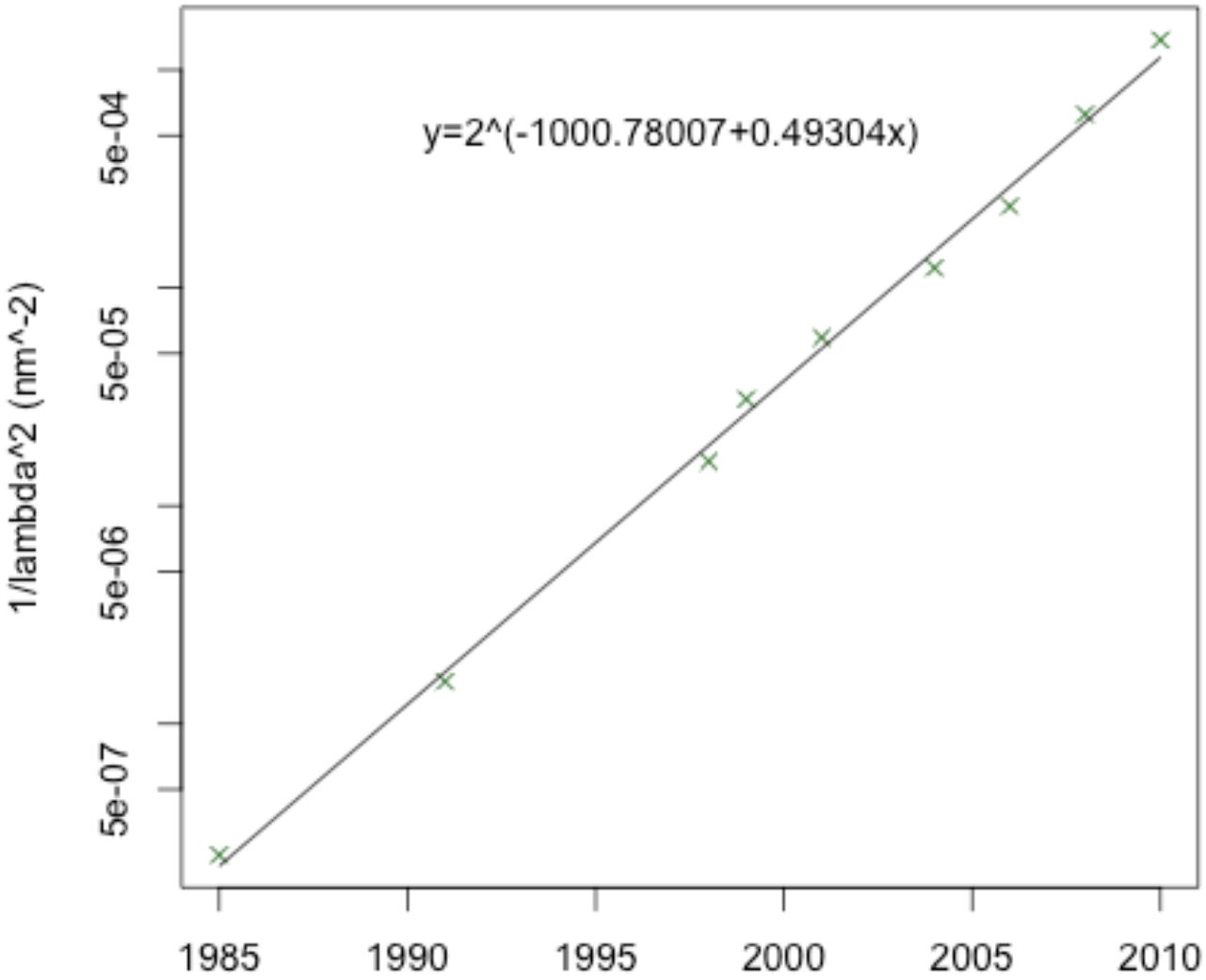
$1/\lambda^2$ vs year

- FPGA lambda from previous table plotted vs year
- Transistor density doubling every two years, in agreement with Moore's Law



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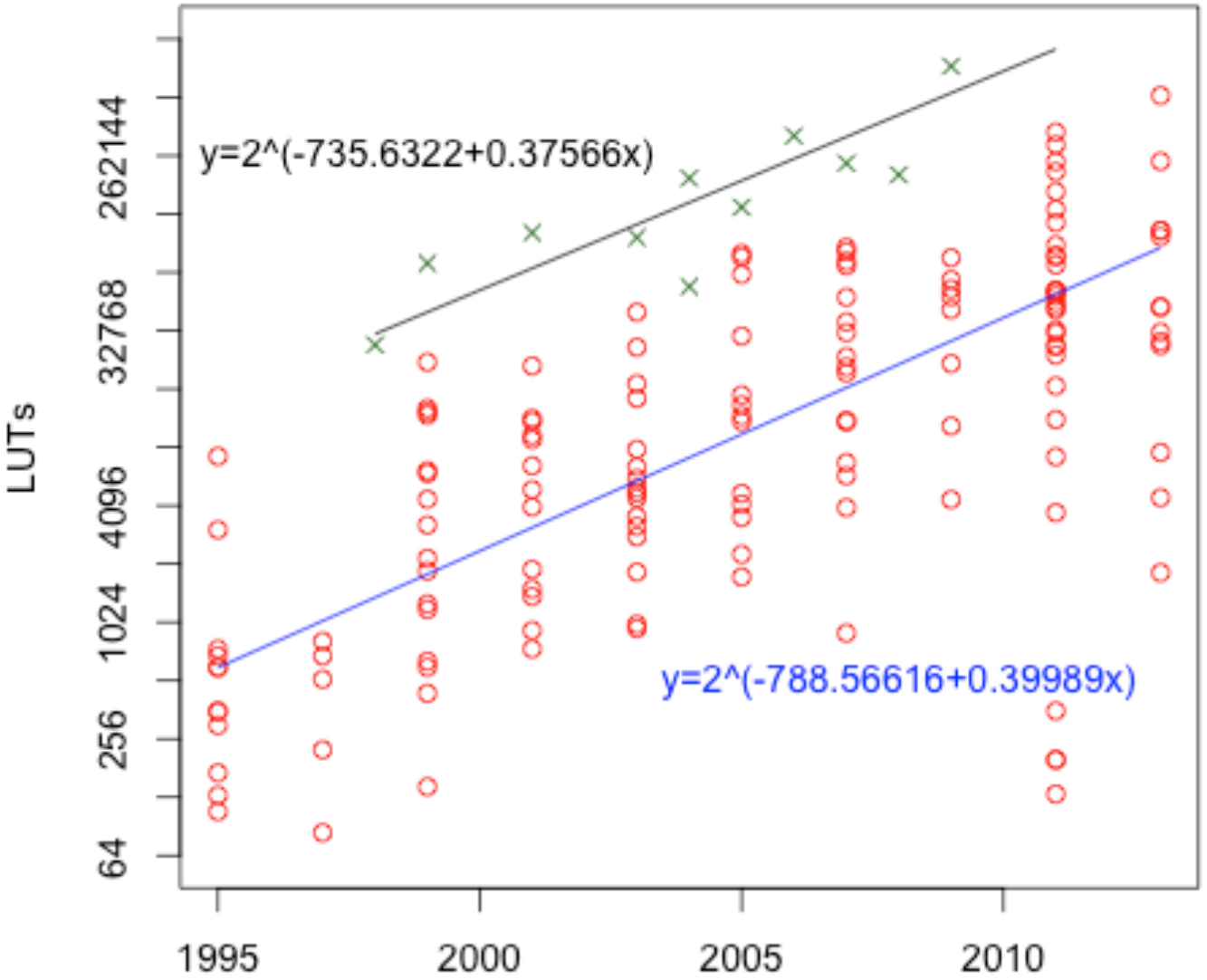
Design Size (number of LUTs)

- x's are the number of LUTs in the largest FPGA of that year
- o's are FCCM designs
- Tech design size doubles every 2.5 years (slightly slower than Moore's Law)
- Inaccuracies because we don't count clock trees and hard blocks



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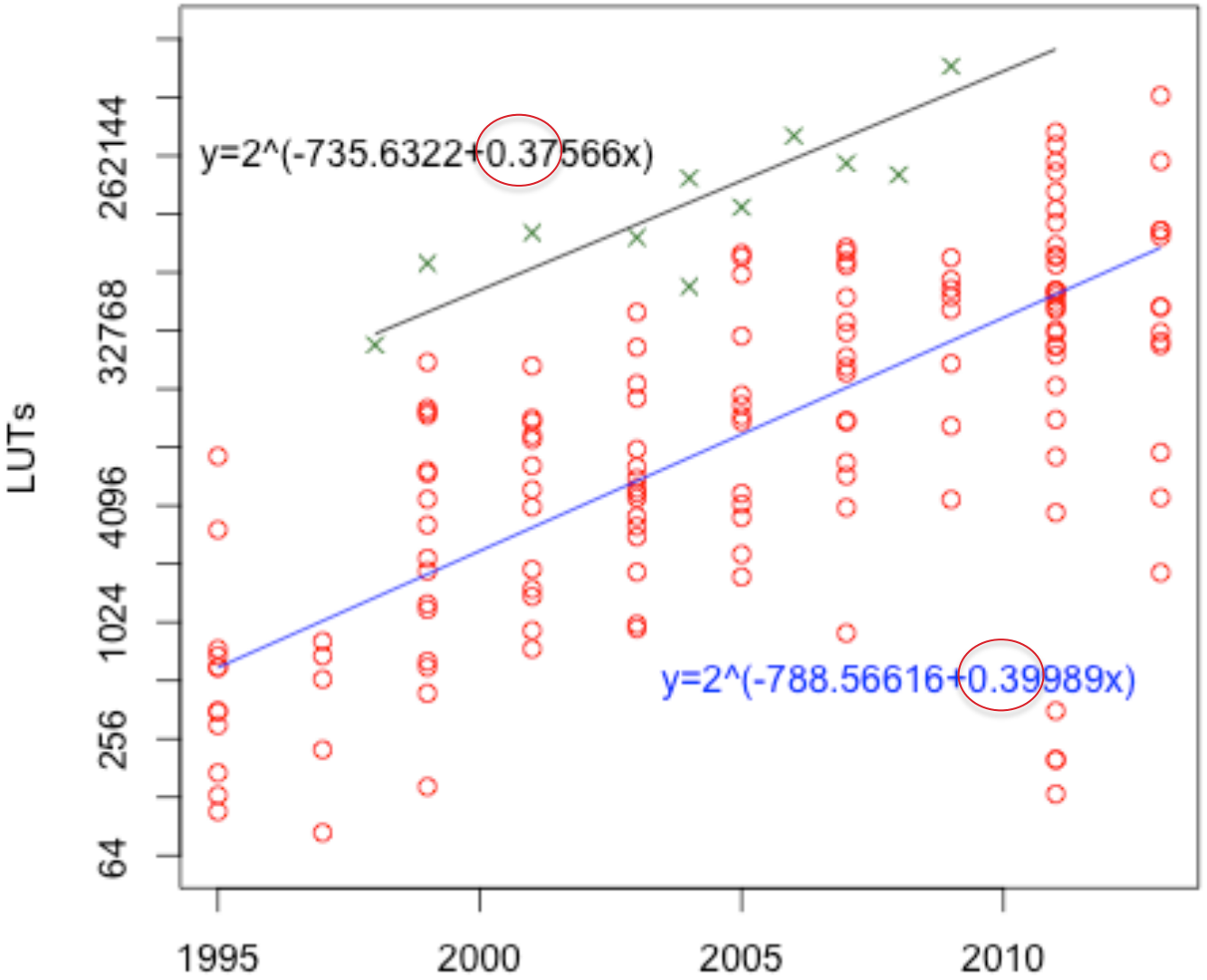

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BRAM Usage

- Tech doubles every 1.8 years
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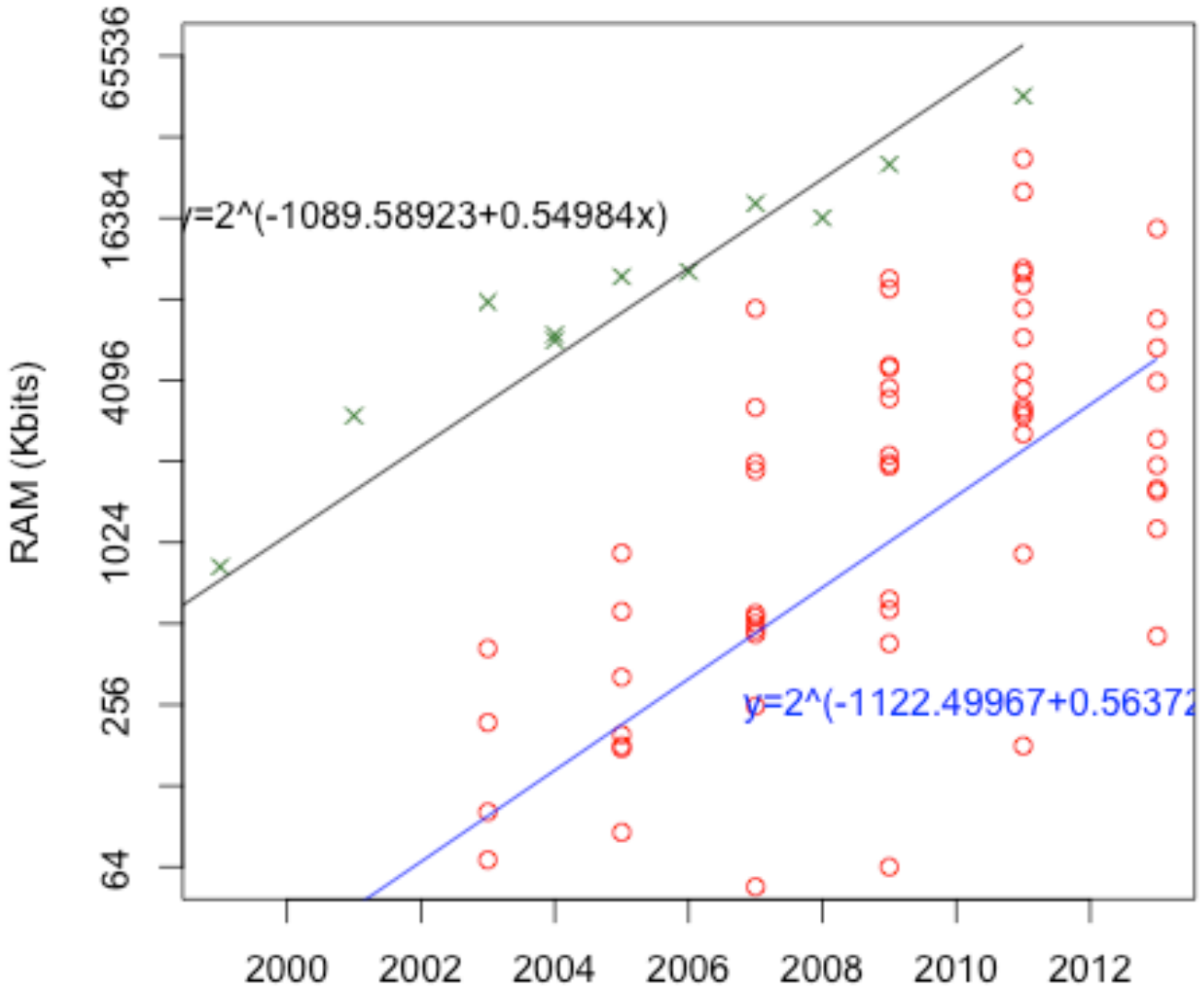
- General trend consistent with Moore's Law



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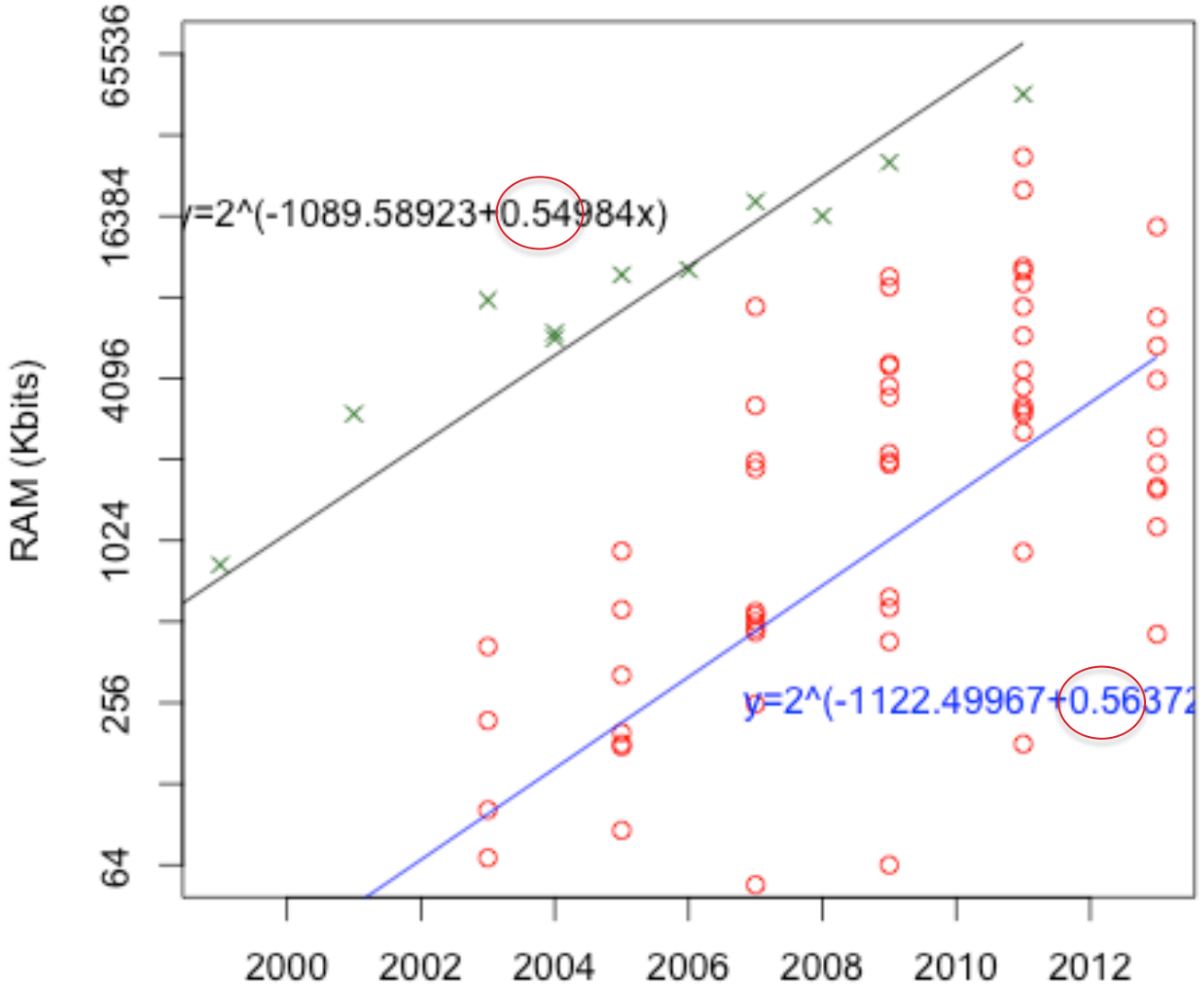

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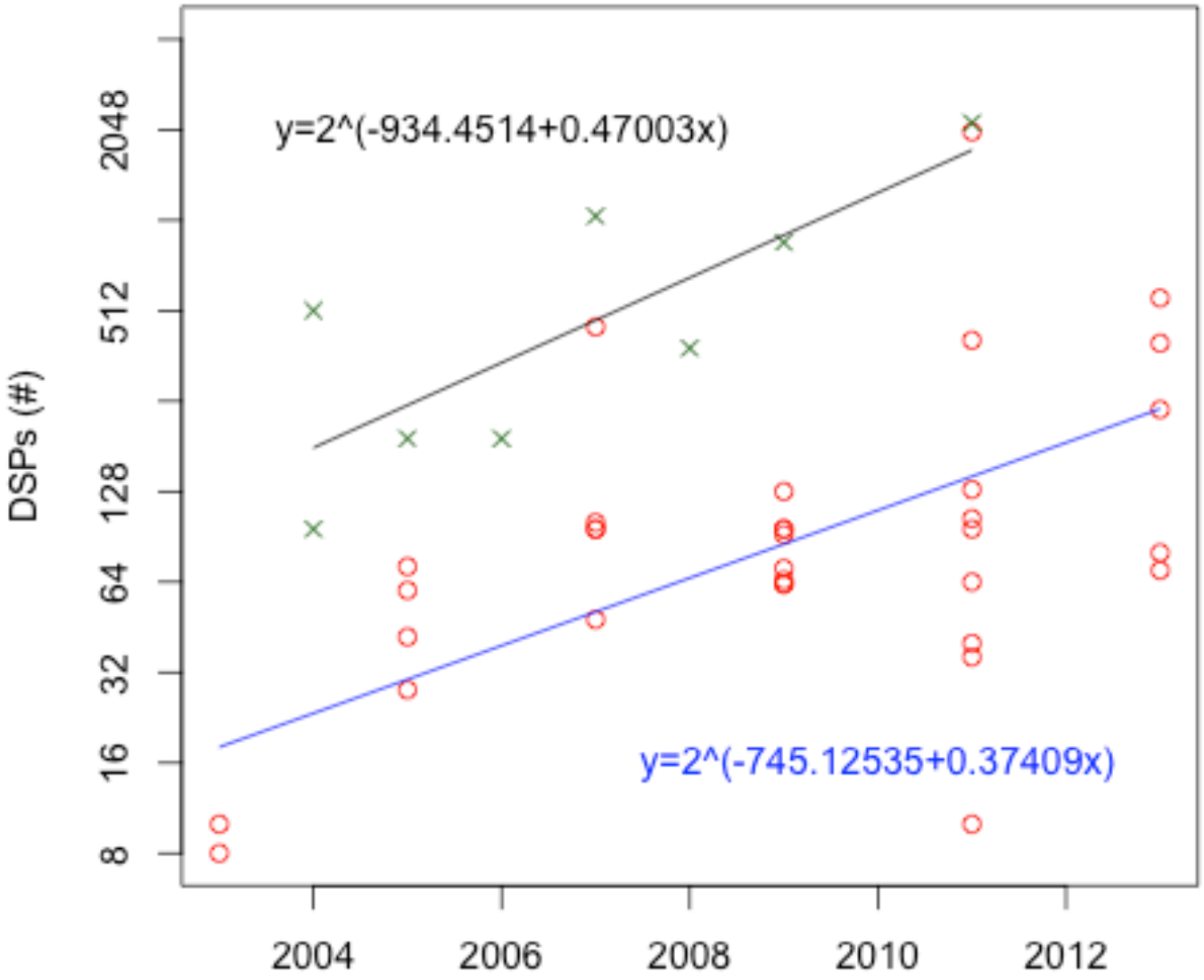
- In some designs DSPs not used or not limiting factor



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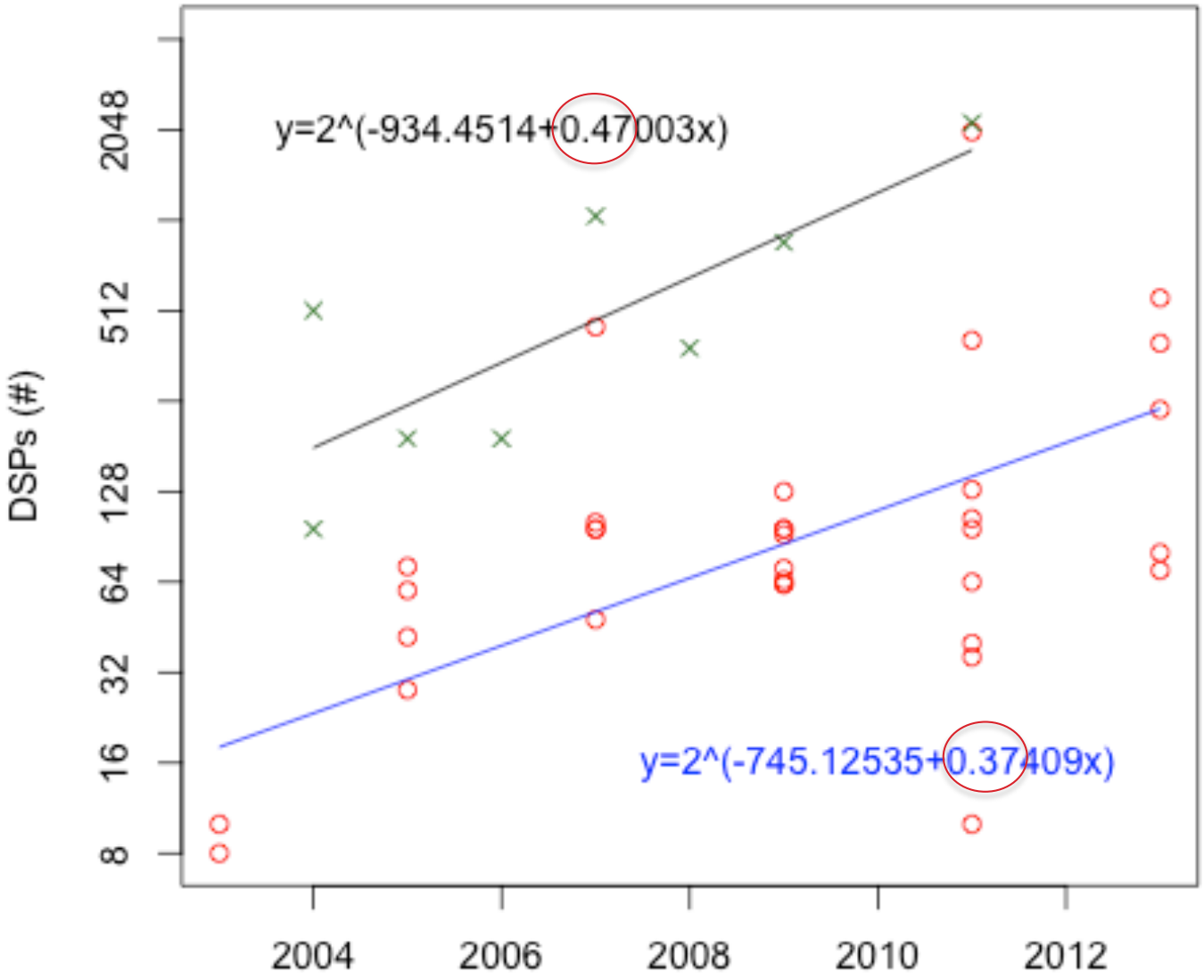

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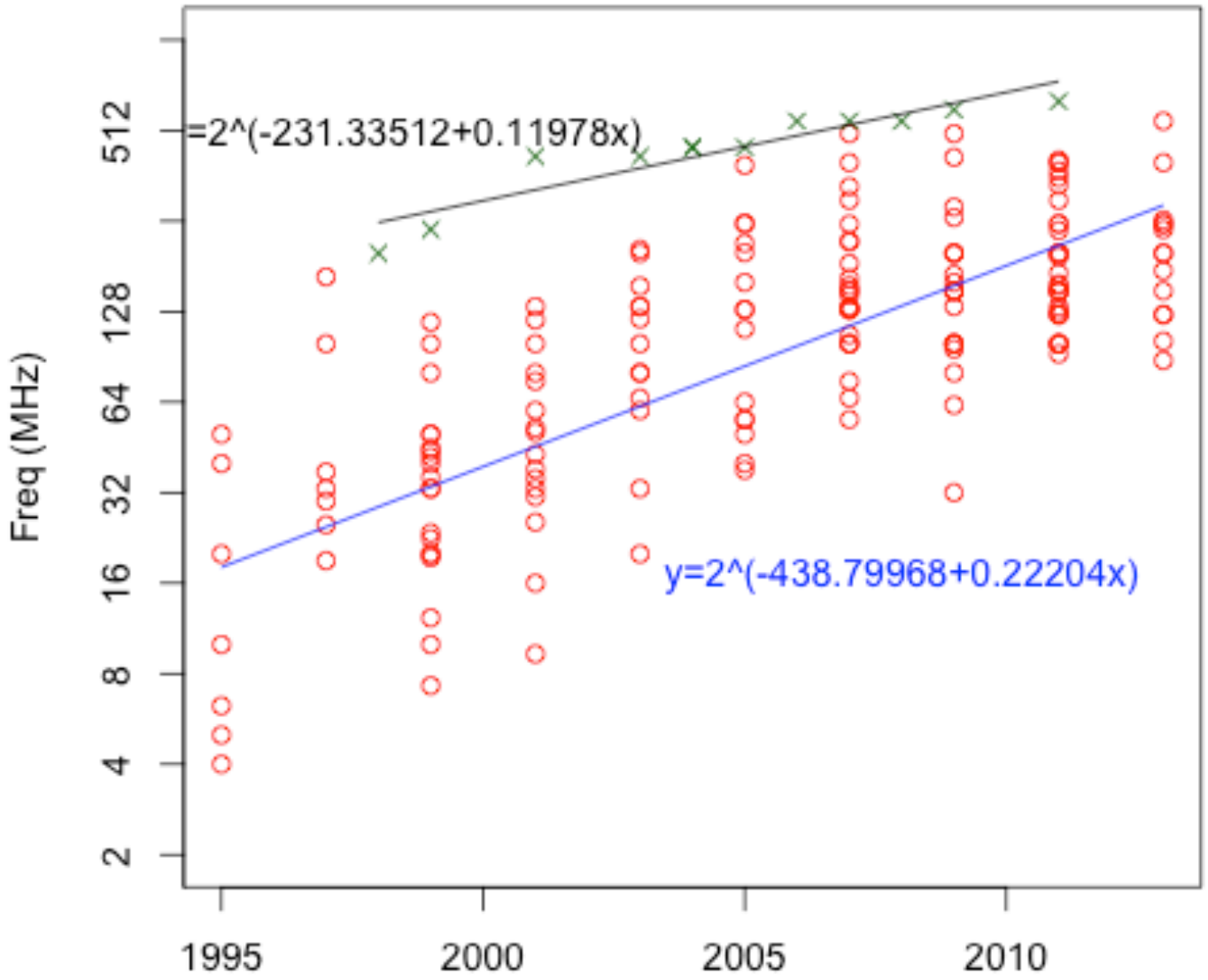
Clock Frequency

- Tech freq doubles every 8 years
- Research freq doubles every 5 years
- Expect doubling every 4 years from Dennard
- Maybe due to hard blocks pushing up frequencies



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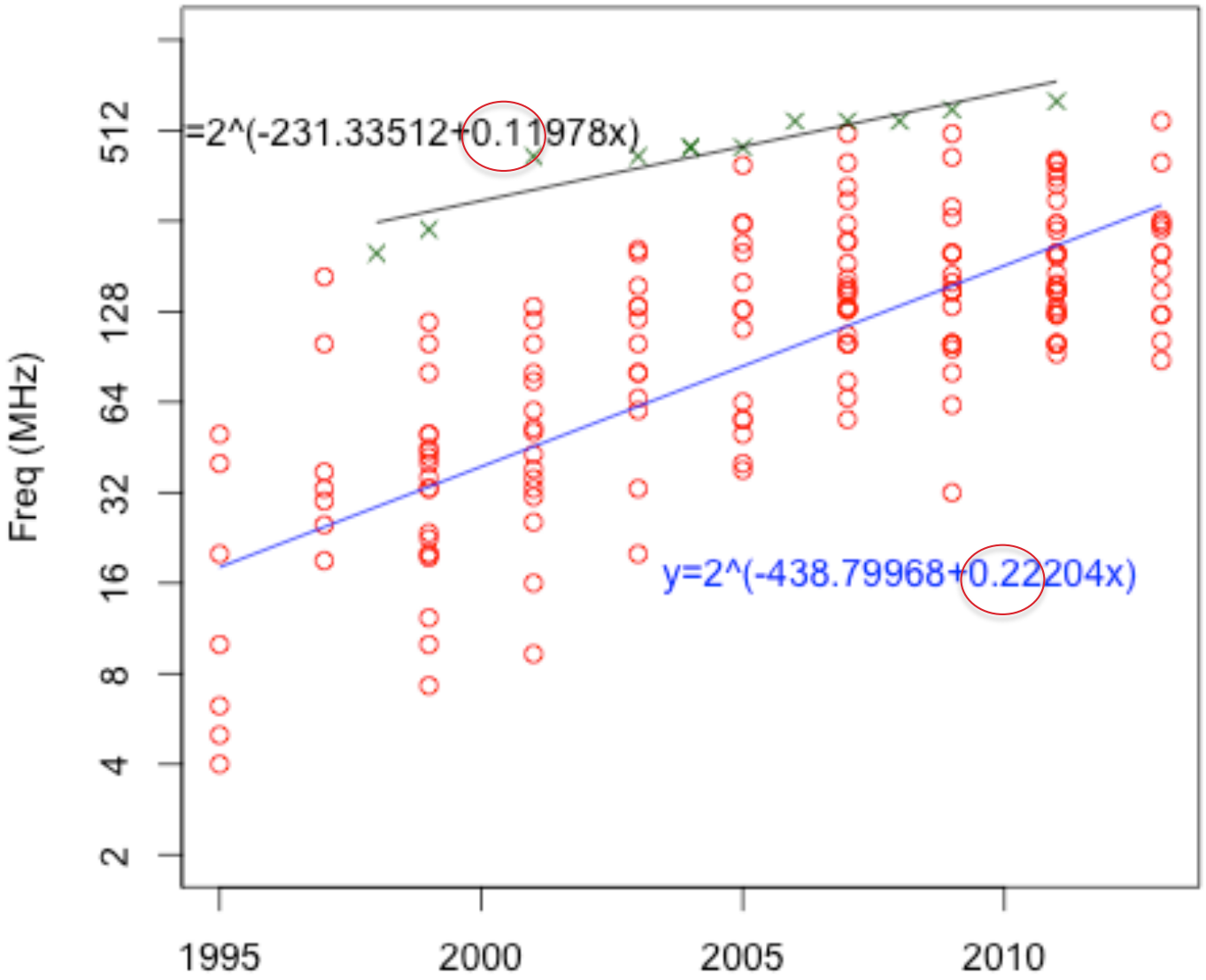

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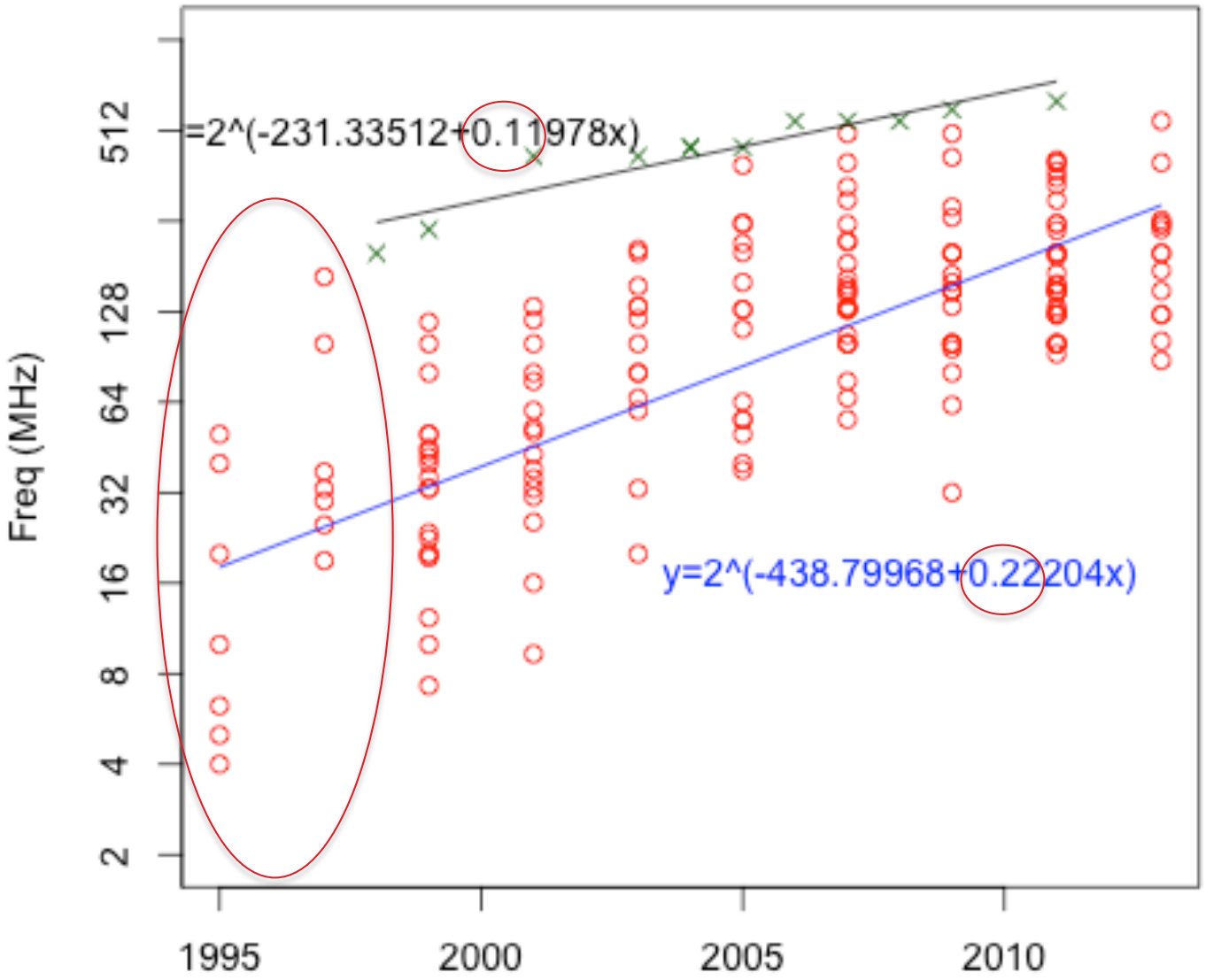
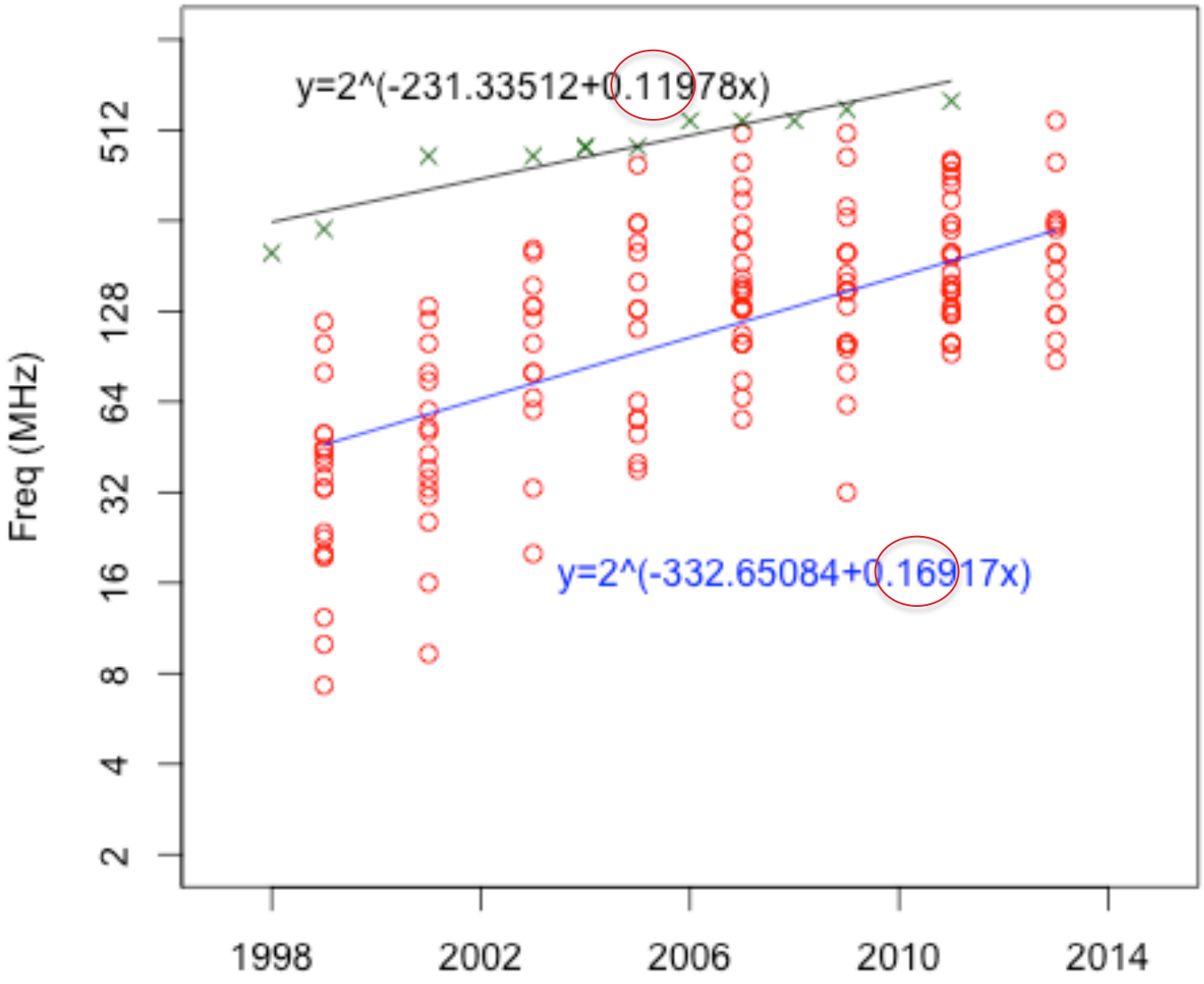
- Note tech trends start from a high value so line is flatter



Clock Frequency (1999-2013)

- **Tech freq doubles every 8 years**
- **Research freq doubles every *6* years**
- Tracking much better with what might be expected based on technology scaling



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How does the model track

› How did we do for 2015?

- Sample designs are from the Applications Session

	4-LUTs (Normalised)	BRAMs (kBits)	DSPs	Operating Frequency	Operating Frequency (updated)
FCCM 2015 data from Apps session (median points)	130536	13338	420	232MHz	232MHz
Predicted	151840	10780	406	390MHz	300MHz
Relative Error (%)	16%	-19%	-3%	68%	29%

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Conclusions

- Quantitative study of 20 years of FCCM designs
  - FPGA feature size closely following Moore's Law
  - # lookup tables for research designs and devices doubling every 2.5 years
  - Design and device operating frequency double in 8 and 5 years respectively, slower than that offered by technology scaling
  - Memory utilization of designs and devices doubling every 1.8 years
  - # DSPs increasing at a faster rate than research designs

Conclusions

- Abovementioned trends can be modeled using the equations introduced
  - In the tradition of FCCM, here's a prediction for the median number of used LUTS used in designs for 2025:

$$y=2^{(-788.56616+0.39989 * 2025)} = \textbf{\textit{2,427K}}$$

- All data available from: http://www.ee.usyd.edu.au/~phwl/UserFiles/File/misc/trends_fccm15.zip

(link also available in paper)

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Future Work

- More detailed determination of normalization factors
- Hypothesized hard blocks are a major factor but not studied
- Do similar studies for different designs, parameters and hard blocks (particularly Rent's Rule and power consumption)
- Use information from research designs to develop better architectures
- Compare these predictions with actual data in the future

Questions?

Thank you for listening