FCCM 2014 Advance Program

Workshops and Reception (Sunday May 11)

Xilinx Workshop

2:00:00 PM	Registration	
2:45:00 PM	Welcoming Remarks	
3:00:00 PM	Domain Customized Languages Workshop	
7:00:00 PM	**FCCM 2014 OPENING RECEPTION**	

DAY 1 (Monday May 12)

7:45:00 AM	Breakfast and Registration	
8:40:00 AM	Welcoming remarks	
	Monday morning, Session 1 **FPGA Synthesis and CGRAs**	
9:00:00 AM	Separation Logic-Assisted Code Transformations for Efficient High-Level Synthesis	Felix Winterstein, Samuel Bayliss and George A. Constantinides
9:20:00 AM	A Fully Pipelined and Dynamically Composable Architecture of CGRA	Jason Cong, Hui Huang, Chiyuan Ma, Bingjun Xiao and Peipei Zhou
9:40:00 AM	Reducing Processing Latency with a Heterogeneous FPGA-Processor Framework	Jonathon Pendlum, Miriam Leeser and Kaushik Chowdhury
9:45:00 AM	Integrated CUDA-to-FPGA Synthesis with Network-on-Chip	Swathi Gurumani, Jacob Tolar, Yao Chen, Yun Liang, Kyle Rupnow and Deming Chen
9:50:00 AM	GraphGen: An FPGA Framework for Vertex-Centric Graph Computation	Eriko Nurvitadhi, Gabriel Weisz, Yu Wang, Skand Hurkat, Marie Nguyen, James C. Hoe, José F. Martinez and Carlos Guestrin
9:55:00 AM	**Poster Session I**	
	Monday morning, Session 2 **Algorithms, Architectures and Circuits for Mathematical Computation**	
11:00:00 AM	A High Memory Bandwidth FPGA Accelerator for Sparse Matrix-Vector Multiplication	Jeremy Fowers, Kalin Ovtcharov, Karin Strauss, Eric Chung and Greg Stitt
11:20:00 AM	A New Algorithm for Carry-Free Addition of Binary Signed-Digit Numbers	Klaus Schneider and Adrian Willenbücher
11:40:00 AM	On Hard Adders and Carry Chains in FPGAs	Jason Luu, Conor McCullough, Sen Wang, Safeen Huda, Bo Yan, Charles Chiasson, Kenneth B. Kent, Jason Anderson, Jonathan Rose and Vaughn Betz
12:00:00 PM	Breaking Sequential Dependencies in FPGA-Based Sparse LU Factorization	Siddhartha and Nachiket Kapre
12:05:00 PM	An Efficient Architecture for Floating-Point Eigenvalue Decomposition	Xinying Wang and Joseph Zambreno
12:10:00 PM	3D FFTs on a Single FPGA	Benjamin Humphries, Hansen Zhang, Jiayi Sheng, Raphael Landaverde, and Martin Herbordt
12:15:00 PM	**Lunch**	
	Monday afternoon, Session 3 **Circuit Characterization and Debug**	
1:45:00 PM	Rapid Post-Map Insertion of Embedded Logic Analyzers for Xilinx FPGAs	Brad Hutchings and Jared Keeley
2:05:00 PM	System-Level Retiming and Pipelining	Girish Venkataramani and Yongfeng Gu
2:25:00 PM	GROK-INT: Generating Real On-chip Knowledge for Interconnect Delays Using Timing Extraction	Benjamin Gojman and André DeHon
2:45:00 PM	Timing Fault Detection in FPGA-Based Circuits	Edward Stott, Joshua M. Levine, Peter Y.K. Cheung and Nachiket Kapre
2:50:00 PM	**Poster Session II**	
	Monday afternoon, Session 4 **Computing and Multi-FPGA Platforms**	

3:50:00 PM	FPGAs in the Cloud: Booting Virtualized Hardware Accelerators with OpenStack	Stuart Byma, J. Gregory Steffan, Hadi Bannazadeh, Alberto Leon-Garcia and Paul Chow
4:10:00 PM	LEAP Shared Memories: Automating the Construction of FPGA Coherent Memories	Hsin-Jung Yang, Kermin Fleming, Michael Adler and Joel Emer
4:30:00 PM	Performance Comparison between Multi-FPGA Prototyping Platforms: Hardwired Off-the-Shelf, Cabling and Custom	Qingshan Tang, Matthieu Tuna and Habib Mehrez
4:50:00 PM	Close Day 1 of Sessions	
6:30:00 PM	**Demo Night and Conference Dinner**	
9:00:00 PM	**Demo Night / Dinner Ends**	
	DAY 2 (Tuesday May 13)	
7:45:00 AM	Breakfast and Registration	
	Tuesday, morning Session 5 **Applications**	
8:40:00 AM	Fast, Power-Efficient Biophotonic Simulations for Cancer Treatment Using FPGAs	Jeffrey Cassidy, Lothar Lilge and Vaughn Betz
9:00:00 AM	SMCGen: Generating Reconfigurable Design for Sequential Monte Carlo Applications	Thomas C.P. Chau, Maciej Kurek, James Stanley Targett, Jake Humphrey, Georgios Skouroupathis, Alison Eele, Jan Maciejowski, Benjamin Cope, Kathryn Cobden, Philip Leong, Peter Y.K. Cheung and Wayne Luk
9:20:00 AM	FPGA Gaussian Random Number Generators with Guaranteed Statistical Accuracy	David B. Thomas
9:40:00 AM	FPGA Implementation of EM Algorithm for 3D CT Reconstruction	Young-Kyu Choi, Jason Cong and Di Wu
9:45:00 AM	A Scalable Multi-engine Xpress9 Compressor with Asynchronous Data Transfer	Joo-Young Kim, Scott Hauck and Doug Burger
9:50:00 AM	FPGA Accelerated Online Boosting for Multi-target Tracking	Matthew Jacobsen, Pingfan Meng, Siddarth Sampangi and Ryan Kastner
9:55:00 AM	**Poster Session III**	
	Tuesday, morning Session 6 **Synthesis II**	
11:00:00 AM	Speeding Up FPGA Placement: Parallel Algorithms and Methods	Matthew An, J. Gregory Steffan and Vaughn Betz
11:20:00 AM	Floorplanning for Partially-Reconfigurable FPGA Systems via Mixed-Integer Linear Programming	Marco Rabozzi, John Lillis and Marco D. Santambrogio
11:40:00 AM	A Grammar Induction Method for Clustering of Operations in Complex FPGA Designs	Muhsen Owaida, Christos D. Antonopoulos and Nikolaos Bellas
12:00:00 PM	Automated Partial Reconfiguration Design for Adaptive Systems with CoPR for Zynq	Kizheppatt Vipin and Suhaib A. Fahmy
12:05:00 PM	MixFX-SCORE: Heterogeneous Fixed-Point Compilation of Dataflow Computations	Deheng Ye and Nachiket Kapre
12:10:00 PM	Automating Optimization of Reconfigurable Designs	Maciej Kurek, Tobias Becker, Thomas C.P. Chau and Wayne Luk
12:15:00 PM	**Lunch**	
	Tuesday afternoon, Session 7 **Energy and Encryption**	
1:45:00 PM	Kung Fu Data Energy - Minimizing Communication Energy in FPGA Computations	Edin Kadric, Kunal Mahajan and André DeHon
2:05:00 PM	Reconstructing AES Key Schedules from Decayed Memory with FPGAs	Heinrich Riebler, Tobias Kenter, Christian Plessl and Christoph Sorge
2:25:00 PM	Low Power Reconfigurable Controllers for Wireless Sensor Network Nodes	Vivek D. Tovinakere, Olivier Sentieys, Steven Derrien and Christophe Huriaux
2:30:00 PM	**Poster Session IV**	
	Tuesday afternoon, Session 8 **Reliability**	
3:30:00 PM	Energy Reduction through Differential Reliability and Lightweight Checking	Edin Kadric, Kunal Mahajan and André DeHon
3:50:00 PM	A Self-Adaptive SEU Mitigation System for FPGAs with an Internal Block RAM Radiation Particle Sensor	Robért Glein, Bernhard Schmidt, Florian Rittner, Jürgen Teich and Daniel Ziener
4:10:00 PM	Look-up Table Design for Deep Sub-threshold through Full-Supply Operation	Monther Abusultan and Sunil Khatri

4:30:00 PM	Best Paper Award, Closing Remarks	
4:50:00 PM	Close conference	
	Poster Session I	
	Using Multi-op Instructions as a Way to Generate ASIPs with Optimized Pipeline Structure	Yosi Ben Asher, Irina Lipov, Vladislav Tartakovsky and Dror Tiv
	A Framework for Dynamic Parallelization of FPGA-Accelerated Applications	Jeremy Fowers, Jianye Liu and Greg Stitt
	Integrated CUDA-to-FPGA Synthesis with Network-on-Chip	Swathi T. Gurumani, Jacob Tolar, Yao Chen, Eric Yun Liang, Kyle Rupnow and Deming Chen
	FPGA Architecture Enhancements to Support Heterogeneous Partially Reconfigurable Regions	Christophe Huriaux, Olivier Sentieys and Russell Tessier
	Customizable Compression Architecture for Efficient Configuration in CGRAs	Syed M.A.H. Jafri, Muhammad Adeel Tajammul, Masoud Daneshtalab, Ahmed Hemani, Kolin Paul, Peeter Ellervee, Juha Plosila and Hannu Tenhunen
	Exploiting Outer Loop Parallelism of Nested Loop on Coarse-Grained Reconfigurable Architectures	Dajiang Liu, Shouyi Yin, Leibo Liu and Shaojun Wei
	Mapping Tasks to a Dynamically Reconfigurable Coarse Grained Array	Mansureh S. Moghaddam, Kolin Paul and M Balakrishnan
	GraphGen: An FPGA Framework for Vertex-Centric Graph Computation	Eriko Nurvitadhi, Gabriel Weisz, Yu Wang, Skand Hurkat, Marie Nguyen, James C. Hoe, José F. Martinez and Carlos Guestrin
	Reducing Processing Latency with a Heterogeneous FPGA-Processor Framework	Jonathon Pendlum, Miriam Leeser and Kaushik Chowdhury
	Better-Than-DMR Techniques for Yield Improvement	Shunichi Sanae, Yuko Hara-Azumi, Shigeru Yamashita and Yasuhiko Nakashima
	A Multi-phase Clock Time-to-Digital Convertor Based on ISERDES Architecture	Tian Xiang, Lei Zhao, Xi Jin, Tianqi Wang, Shaoping Chu, Cong Ma, Shubin Liu, Qi An and Xue Ben
	Poster Session II	
	Design Space Exploration to Accelerate Nelder-Mead Algorithm Using FPGA	Nam Khanh Pham, Amit Kumar Singh, Akash Kumar, and Khin Mi Mi Aung
	Experiments in Mapping Expressions to DSP Blocks	Ronak Bajaj and Suhaib A. Fahmy
	Memory Optimized Re-gridding for Non-uniform Fast Fourier Transform on FPGAs	Umer I. Cheema, Gregory Nash, Rashid Ansari, and Ashfaq A. Khokhar
	Reducing Overheads for Fault-Tolerant Datapaths with Dynamic Partial Reconfiguration	James J. Davis and Peter Y.K. Cheung
	Accelerator of Stacked Convolutional Independent Subspace Analysis for Deep Learning-Based Action Recognition	Lu He, Yan Luo and Yu Cao
	Building Optimized Packet Filters with COFFi	Sven Hager, Frank Winkler, Björn Scheuermann and Klaus Reinhardt
	3D FFTs on a Single FPGA	Benjamin Humphries, Hansen Zhang, Jiayi Sheng, Raphael Landaverde, and Martin C. Herbordt
	From GPU to FPGA: A Pipelined Hierarchical Approach to Fast and Memory-Efficient NDN Name Lookup	Yanbiao Li, Dafang Zhang, Xian Yu, Jing Long and Wei Liang
	Timing Fault Detection in FPGA-Based Circuits	Edward Stott, Joshua M. Levine, Peter Y.K. Cheung, and Nachiket Kapre
	High-Throughput Fixed-Point Object Detection on FPGAs	Xiaoyin Ma, Walid Najjar and Amit Roy-Chowdhury
	UTOPIA: Generic User-Level Access to the Physical Memory Address Space for IP Core Debugging and Validation on FPGA Based PCIe Extension Cards	Hendrik Nöll, Sebastian Siegert, Johannes Hiltscher, and Wolfgang Rehm
	Breaking Sequential Dependencies in FPGA-Based Sparse LU Factorization	Siddhartha and Nachiket Kapre
	An Efficient Architecture for Floating-Point Eigenvalue Decomposition	Xinying Wang and Joseph Zambreno
	Poster Session III	
	An Architectural Approach to Characterizing and Eliminating Sources of Inefficiency in a Soft Processor Design	Kaveh Aasaraai and Andreas Moshovos
	Abstract: Shared L2 Cache Management in Multicore Real-Time System	Gang Chen, Biao Hu, Kai Huang, Alois Knoll, Kai Huang and Di Liu
	FPGA Implementation of EM Algorithm for 3D CT Reconstruction	Young-Kyu Choi, Jason Cong and Di Wu
	FPGA Accelerated Online Boosting for Multi-target Tracking	Matthew Jacobsen, Pingfan Meng, Siddarth Sampangi and Ryan Kastner
	Harmonica: An FPGA-Based Data Parallel Soft Core	Chad Kersey, Sudhakar Yalamanchili, Hyojong Kim, Nimit Nigania, and Hyesoon Kim

A Scalable Multi-engine Xpress9 Compressor with Asynchronous Data Transfer	Joo-Young Kim, Scott Hauck and Doug Burger
FPGA Acceleration for Simultaneous Medical Image Reconstruction and Segmentation	Peng Li, Thomas Page, Guojie Luo, Wentai Zhang, Pei Wang, Peng Zhang, Peter Maass, Ming Jiang and Jason Cong
A Hierarchical Memory Architecture with NoC Support for MPSoC on FPGAs	Shiming Li, Miaoqing Huang, Hongyuan Ding and Sen Ma
Accurate and Efficient Three Level Design Space Exploration Based on Constraints Satisfaction Optimization Problem Solver	Shuo Li and Ahmed Hemani
Towards an Area-Efficient Implementation of a High ILP EDGE Soft Processor	Aaron Smith and Jan Gray
FPGA Implementation of Optical Flow Algorithm Based on Cost Aggregation	Yu Tanabe and Tsutomu Maruyama
Image Signal Processors on FPGAs	Di Wu and Andreas Moshovos
A Fully-Pipelined FPGA Design for Tree-Reweighted Message Passing Algorithm	Wenlai Zhao, Haohuan Fu and Guangwen Yang
Poster Session IV	
Compiling Higher Order Functional Programs to Composable Digital Hardware	Eduardo Aguilar-Pelaez, Samuel Bayliss, Alex Smith, Felix Winterstein, Dan R. Ghica, David Thomas, and George A. Constantinides
Fast Design-Space Exploration Method for SW/HW Codesign on FPGAs	Yuki Ando, Seiya Shibata, Shinya Honda, Hiroyuki Tomiyama and Hiroaki Takada
Flexibility and Circuit Overheads in Reconfigurable SIMD/MIMD Systems	S. Arrabi, D. Moore, L. Wang, K. Skadron, B.H. Calhoun, J. Lach, and B.H. Meyer
Fast and Power Efficient Heapsort IP for Image Compression Application	Yuhui Bai, Syed Zahid Ahmed and Bertrand Granado
A Hardware MPI Spawn for Distributed Multiprocessing Reconfigurable System on Chip (MP-RSoC)	R. Christian Gamom Ngounou Ewo, Andrea Pinna, Bertrand Granado, Martin Mbouenda, and H. Bertrand Fotsin
MRAPI Implementation for Heterogeneous Reconfigurable Systems-on-Chip	L. Gantel, M.E.A. Benkhelifa, F. Verdier, and F. Lemonnier
Scheduling Mixed-Architecture Processes in Tightly Coupled FPGA-CPU Reconfigurable Computers	Brandon Kyle Hamilton, Michael Inggs, and Hayden Kwok-Hay So
Automating Optimization of Reconfigurable Designs	Maciej Kurek, Tobias Becker, Thomas C.P. Chau, and Wayne Luk
A Power-Efficient FPGA-Based Mixture-of-Gaussian (MoG) Background Subtraction for Full-HD Resolution	Hamed Tabkhi, Majid Sabbagh and Gunar Schirner
Low Power Reconfigurable Controllers for Wireless Sensor Network Nodes	Vivek D. Tovinakere, Olivier Sentieys, Steven Derrien, and Christophe Huriaux
Automated Partial Reconfiguration Design for Adaptive Systems with CoPR for Zynq	Kizheppatt Vipin and Suhaib A. Fahmy
High-Throughput and Low-Cost Hardware Accelerator for Privacy Preserving Publishing	Fumito Yamaguchi and Hiroaki Nishi
MixFX-SCORE: Heterogeneous Fixed-Point Compilation of Dataflow Computations	Deheng Ye and Nachiket Kapre