FCCM 2013 Preliminary Program

The 21st Annual International IEEE Symposium on Field-Programmable Custom Computing Machines
Seattle, Washington USA April 28 -30 2013 www.fccm.org

Sunday, April 28th

12:00 PM	**Registration Opens**
1:00 - 4:00 PM	**Panel Discussion** *Reconfigurable Computing in the Era of Post-Silicon Scaling* Eric Chung (Microsoft Research) and Mike Butts (Nvidia) will co-chair the discussion. A speaker list and additional details will be posted on the FCCM website.
4:00 - 6:00 PM	**Pico Computing Workshop** This tutorial will describe Pico Computing's vision for simplifying FPGA development. Pico provides an FPGA framework and a flexible software API that eliminates the typical boilerplate required to develop accelerated applications and/or perform architectural exploration. This workshop will walk users through the Pico framework and development cycle, demonstrating both the software and HDL required to migrate a compute-intensive software application to an accelerated software/hardware solution.

Monday, April 29th

8:00 AM	**Registration Opens**
8:00 - 9:00 AM	**Continental Breakfast**
9:00 AM	**Opening Remarks**
9:10 AM	**Session 1: Data Drive Computing**
9:10 AM	*Parallel Computation of Skyline Queries* Louis Woods, Jens Teubner and Gustavo Alonso
9:30 AM	*Minerva: Accelerating Data Analysis in Next-Generation SSDs* Arup De, Maya Gokhale, Rajesh Gupta and Steven Swanson
9:50 AM	*Accelerating Join Operation for Relational Databases with FPGAs (short)* Robert Halstead, Bharat Sukhwani, Hong Min, Mathew Thoennes, Parijat Dube, Sameh Asaad and Balakrishna Iyer
9:55 AM	*Boosting Memory Performance of Many-Core FPGA Device through Dynamic Precedence Graph (short)* Yu Bai, Abigail Fuentes, Michael Riera, Mohammed Alawad, and Mingjie Lin
10:00 AM	*Acceleration of SQL Restrictions and Aggregations through FPGA-based Dynamic Partial Reconfiguration (short)* Christopher Dennl, Daniel Ziener and Jürgen Teich
10:05 AM	**Poster Session I and Coffee Break**
11:05 AM	**Session 2: Hardware Considerations**
11:05 AM	*Accuracy-Performance Tradeoffs on an FPGA Through Overclocking* Kan Shi, David Boland and George A. Constantinides
11:25 AM	*Safe Overclocking of Tightly Coupled CGRAs and Processor Arrays Using Razor* Alex Brant, Ameer Abdelhadi, Douglas Sim, Tom Tang, Michael Yue and Guy G.F. Lemieux
11:45 AM	*Escaping the Academic Sandbox: Realizing VPR Circuits on Xilinx Devices* Eddie Hung, Fatemeh Eslamy and Steven J. E. Wilton

12:05 PM	*Heterogeneous Technology-Mapping: Soft versus Hard Multiplexers (short)* Madhura Purnaprajna and Paolo Ienne
12:10 PM	*PAMPER: Precomputed Alternatives for Mitigating Parametric-variation Energy via Reconfiguration (short)* Raphael Rubin, Nikil Mehta and André DeHon
12:15 PM	*Accurate Thermal-Profile Estimation and Validation for FPGA-Mapped Circuits (short)* Abdulazim Amouri, Hussam Amrouch, Thomas Ebi, Jörg Henkel and Mehdi Tahoori
12:20 PM	*On-chip Context Save and Restore of Hardware Tasks on Partially Reconfigurable FPGAs (short)* Aurelio Morales-Villanueva and Ann Gordon-Ross
12:25 PM	**Lunch**
2:10 PM	**Session 3: Applications I**
2:10 PM	*A High Throughput No-Stall Golomb-Rice Hardware Decoder* Roger Moussalli, Walid Najjar, Xi Luo and Amna Khan
2:30 PM	*Image Segmentation Using Hardware Forest Classifiers* Neil Pittman, Alessandro Forin, Atabak Mahram, Antonio Criminisi and Jamie Shotton
2:50 PM	*A Reconfigurable Architecture for 1-D and 2-D Discrete Wavelet Transform (short)* Qing Sun, Jiang Jiang, Yongxin Zhu, Yuzhuo Fu
2:55 PM	*High Speed Video Processing Using Fine-Grained Processing on FPGA Platform (short)* Zhi Ping Ang, Akash Kumar and Yajun Ha
3:00 PM	**Poster Session II and Coffee Break**
4:00 PM	**Session 4: Tools**
4:00 PM	*The Effect of Compiler Optimizations on High-Level Synthesis for FPGAs* Qijing Huang, Ruolong Lian, Andrew Canis, Jongsok Choi, Ryan Xi, Stephen Brown and Jason Anderson
4:20 PM	*Automating Resource Optimization in Reconfigurable Design* Xinyu Niu, Thomas Chau, Qiwei Jin, Wayne Luk and Qiang Liu
4:40 PM	*Open-Source Bitstream Generation* Ritesh Kumar Soni, Neil Steiner and Matthew French
5:00 PM	*ShrinkWrap: Compiler-Enabled Optimization and Customization of Soft Memory Interconnects (short)* Eric Chung and Michael Papamichael
5:05 PM	*PRML: A Modeling Language for Rapid Design Exploration of Partially Reconfigurable FPGAs (short)* Rohit Kumar and Ann Gordon-Ross
6:00 PM	**Demo Night Banquet** This informal show-and-tell over dinner and drinks is a long standing and exciting FCCM tradition. All attendees are welcome to bring hardware and software to display! Simply register (shepard.siegel at atomicrules.com) and we will provide space at Monday's event. This is a great free opportunity to discuss your work with attendees in a relaxed setting! During the event, we will also take time to honor 20 years of FCCM by presenting awards to the authors and papers selected to appear in our FCCM20 highlights volume. All attendees will receive this special-edition Proceedings, containing the most significant papers presented at the conference through the years.

Tuesday, April 30th

8:00 AM	**Registration Opens**
8:00 - 9:00 AM	**Solarflare University Program Breakfast** Start your day right with Solarflare's Breakfast Reception! Learn about Solarflare's new University Program that provides FPGA-based products for classroom instruction in Computer Science and Computer Engineering and enables Computer Science researchers to pioneer advances in Custom Compute through the use of Solarflare's AOE (ApplicationOnload Engine) hardware and development kits. For more information on Solarflare's University Program, please visit http://www.solarflare.com/University-Program
9:00 AM	**Session 5: Networking**
9:00 AM	*Atacama: An Open FPGA-based Platform for Mixed-Criticality Communication in Multi-Segmented Ethernet Networks* Gonzalo Carvajal, Sebastian Fischmeister, Miguel Figueroa and Robert Trausmuth
9:20 AM	*Latency-Optimized Networks for Clustering FPGAs* Trevor Bunker and Steven Swanson
9:40 AM	*A Range and Scaling Study of an FPGA-based Digital Wireless Channel Emulator* Scott Buscemi, Will Kritikos and Ron Sass
10:00 AM	*Enabling Hardware Exploration in Software-Defined Networking: A Flexible, Portable OpenFlow Switch (short)* Asif Khan and Nirav Dave
10:05 AM	*An FPGA based PCIE Root Complex Architecture for Standalone SOPCs (short)* Yingjie Cao, Yongxin Zhu, Xu Wang, Jiang Jiang and Meikang Qiu
10:10 AM	**Poster Session III and Coffee Break**
11:10 AM	**Session 6: Applications II**
11:10 AM	*Application Composition and Communication Optimization of Iterative Solvers using FPGAs* Abid Rafique, Nachiket Kapre and George Constantinides
11:30 AM	*Parallel generation of Gaussian random numbers using the Table-Hadamard transform* David Thomas
11:50 AM	*Hardware-Software Codesign for Embedded Numerical Accelerators (short)* Ranko Sredojevic, Andrew Wright and Vladimir Stojanovic
11:55 AM	*FAssem : FPGA based Acceleration of De Novo Genome Assembly (short)* Sharat Chandra Varma Bogaraju, Paul Kolin, M Balakrishnan and Dominique Lavenier
12:00 PM	*Accelerating the Computation of Induced Dipoles for Molecular Mechanics with Dataflow Engines (short)* Frederico Pratas, Diego Oriato, Oliver Pell, Ricardo Mata and Leonel Sousa
12:05 PM	**Lunch**
1:30 PM	**Session 7: Arithmetic**
1:30 PM	*On optimizing the arithmetic precision of MCMC algorithms* Grigorios Mingas, Farhan Rahman and Christos-Savvas Bouganis
1:50 PM	*Exploiting Input Parameter Uncertainty for Reducing Datapath Precision of SPICE Device Models* Nachiket Kapre
2:10 PM	*Efficient Large Integer Squarers on FPGA (short)* Simin Xu, Suhaib A Fahmy and Ian V McLoughlin

2:15 PM	*Elementary Function Implementation with Optimized Sub Range Polynomial Evaluation (short)* Martin Langhammer and Bogdan Pasca
2:20 PM	*High-Level Description and Synthesis of Floating-Point Accumulators on FPGA (short)* Marc-Andre Daigneault and Jean Pierre David
2:25 PM	**Poster Session IV and Coffee Break**
3:30 PM	**Session 8: Applications II**
3:30 PM	*Reconfigurable Acceleration of Short Read Mapping* James Arram, Kuen Hung Tsoi and Wayne Luk
3:50 PM	*An FPGA-Based Data Flow Engine For Gaussian Copula Model* Huabin Ruan, Xiaomeng Huang, Guangwen Yang, Haohuan Fu, Sebastien Racaniere, and Oliver Wenjing
4:10 PM	**Wrap Up and Best Paper Awards**