FCCM 2011 Program

Sunday, May 1, 2011

1:30pm **FCCM Workshop** (Officer's Club)
High-level Synthesis and Parallel Computation Models

Kyle Rupnow, Advanced Digital Sciences Center (ADSC), Singapore**,** Satnam Singh, Microsoft Research**,** John Wawrzynek, UC Berkeley

6:00pm **Opening Reception** (Pierre Lassonde House)

Monday, May 2, 2011

8:00am **Registration Opens** (Officer's Club)

8:30am **Opening Remarks**

8:45am **Monday morning, Session 1:**
Reconfigurable Computing
Session Chairs: Andre' DeHon and Ken Eguro

A Sparse Matrix Personality for the Convey HC-1
Krishna K. Nagar and Jason D. Bakos
University of South Carolina

Modeling Dynamically Reconfigurable Systems for Simulation-based Functional Verification
Lingkan Gong and Oliver Diessel
University of New South Wales

Mixed Precision Processing in Reconfigurable Systems
[1]*Gary C.T. Chow,* [1]*K.W. Kwok,* [1]*Wayne Luk and* [2]*Philip Leong*
[1]Imperial College London, [2]The University of Sydney

Dynamic Communication in a Coarse Grained Reconfigurable Array (short)
Robin Panda and Scott Hauck
University of Washington

Run-Time Resource Allocation for Simultaneous Multi-Tasking in Multi-Core Reconfigurable Processors (short)
Waheed Ahmed, Muhammad Shafique, Lars Bauer, Manuel Hammerich, Jörg Henkel and Juergen Becker
Karlsruhe Institute of Technology (KIT)

An Autonomous Vector/Scalar Floating Point Coprocessor for FPGAs (short)
Jainik Kathiara and Miriam Leeser
Northeastern University

Hecto-Scale Frame Rate Face Detection System for SVGA Source on FPGA Board (short)
[1]*Zheng Ding,* [2]*Feng Zhao,* [1]*Tinghui Wang,* [1]*Wei Shu and* [1]*Min-You Wu*
[1]Shanghai Jiao Tong University, [2]Digilent Electronic Technology Co. Ltd.

10:15am **Poster Session I**

11:15am **Monday morning, Session 2:**
Comparing Implementations of Applications on Different Architectures
Session Chair: Miriam Leeser

An FPGA implementation of Information Theoretic Visual-Saliency System and Its Optimization
Sungmin Bae, Yong Cheol Peter Cho, Sungho Park, Kevin M. Irick, Yongseok Jin and N. Vijaykrishnan
Pennsylvania State University

Scalable, High Performance Fourier Domain Optical Coherence Tomography: why FPGAs and not GPGPUs
Jian Li, Marinko Sarunic and Lesley Shannon
Simon Fraser University

Architecture, Design, and Experimental Evaluation of a Lightfield Descriptor Depth Buffer Algorithm on Reconfigurable Logic
Matina Lakka, Grigorios Chrysos, Ioannis Papaefstathiou and Apostolos Dollas
Technical University of Crete

Implementation and Performance Analysis of Seal Encryption on FPGA, GPU, and Multicore Processors (short)
Kostas Theoharoulis, Haralambos Antoniadis, Nikolaos Bellas and Christos Antonopoulos
University of Thessaly

12:25pm **Lunch** (Heritage Center)

2:00pm **Monday afternoon, Session 3:**
Applications I
Session Chairs: Jeff Arnold and Mike Butts

Open Source FPGA Communications Framework (short)
Peter Lieber and Brad Hutchings
Brigham Young University

Efficient Calculation of Pairwise Nonbonded Forces (short)

Matt Chiu, Md. Ashfaquzzaman Khan and Martin Herbordt
Boston University

High Performance IP Lookup on FPGA with Combined Length-Infix Pipelined Search (short)
[1]*Yi-Hua E. Yang,* [2]*Oguzhan Erdem and* [1]*Viktor K. Prasanna*
[1]University of Southern California, [2]Middle-East Technical University

A Scalable Multi-FPGA Platform for Complex Networking Applications (short)
[1]*Sascha Mühlbach and* [2]*Andreas Koch*
[1]Center for Advanced Security Research Darmstadt, [2]Technische Universität Darmstadt

An FPGA-based Optical IOH Architecture for Embedded System (short)
Ling Liu, Jincan Zhuang, Qianying Zhu, Shunyu Zhu, Zhiyuan Zhang, Xinxin Zhang, Lu Cao, Zhihong Yu, Xiangbin Wu and Dong Liu
Intel

On Comparing Financial Price Solvers on FPGA (short)
Qiwei Jin, David Thomas and Wayne Luk
Imperial College London

Low-latency FPGA Based Financial Data Feed Handler (short)
[1]*Robin Pottathuparambil,* [2]*Jack Coyne,* [2]*Jeffrey Allred,* [2] *William Lynch and* [2]*Vincent Natoli*
[1]University of North Carolina at Charlotte, [2]Stone Ridge Technology

Design and Implementation of an FPGA-based Real-Time Face Recognition System (short)
Janarbek Matai, Ali Irturk and Ryan Kastner
University of California, San Diego

FPGA-Based Solid-State Drive Prototyping with NAND Flash Memories (short)
[1]*Yu Cai,* [2]*Eric F. Haratsch,* [1]*Mark McCartney and* [1]*Ken Mai*
[1]Carnegie Mellon University, [2]LSI Corporation

Accelerating Statistical LOR Estimation for a High-Resolution PET Scanner using FPGA Devices and a High Level Synthesis Tool (short)
[1]*Zhong-Ho Chen,* [1]*Alvin Su,* [2]*Scott Hauck and* [2]*Ming-Ting Sun*
[1]National Cheng-Kung University, [2]University of Washington

SYSCORE: A Coarse Grained Reconfigurable Array Architecture for Low Energy Biosignal Processing (short)
Kunjan Patel, Chris Bleakley and Seamas McGettrick
University College Dublin

109 **A high-throughput, streaming, lossless data compression algorithm and its efficient hardware implementation**
Bharat Sukhwani, Bulent Abali, Bernard Brezzo and Sameh Asaad
IBM T. J. Watson Research Center

3:00pm **Poster Session II**

4:00pm **Monday afternoon, Session 4:**
Tools
Session Chair: Jason Anderson

HMFlow: Accelerating FPGA Compilation with Hard Macros for Rapid Prototyping
Christopher Lavin, Marc Padilla, Jaren Lamprecht, Philip Lundrigan, Brent Nelson and Brad Hutchings
Brigham Young University

Automatic HDL-based generation of homogeneous hard macros for FPGAs
[1]*Sebastian Korf,* [1]*Dario Cozzi,* [1]*Markus Koester,* [1]*Jens Hagemeyer,* [1]*Mario Porrmann,* [2]*Marco Domenico Santambrogio and* [3]*Ulrich Rückert*
[1]University of Paderborn, Germany, [2]Massachusetts Institute of Technology, USA, [3]University of Bielefeld, Germany

Using Functional Programming to Generate an LDPC Forward Error Corrector
Andy Gill, Tristan Bull, Dan DePardo, Andrew Farmer, Ed Komp and Erik Perrins
University of Kansas

6:30pm **Demo Night (Officer's Club)**

Tuesday, May 3, 2011

8:00am **Registration Opens** (Officer's Club)

8:30am **Tuesday morning, Session 5:**
Reconfigurable Computing in the Data Center (Panel Session)

Reconfigurable Data Processing for Clouds (short)
[1]*Anil Madhavapeddy and* [2]*Satnam Singh*
[1]University of Cambridge, [2]Microsoft Research Cambridge, UK

10:00am **Coffee Break**

10:30am **Tuesday morning, Session 6:**
Architecture and Systems
Session Chair: David Andrews

TMbox: A Flexible and Reconfigurable 16-core Hybrid Transactional Memory System
[1]*Nehir Sonmez,* [1]*Oriol Arcas,* [1]*Otto Pflucker,* [1]*Osman Unsal,* [1]*Adrián Cristal,* [1]*Ibrahim Hur,* [2]*Satnam Singh and* [1]*Mateo Valero*
[1]Barcelona Supercomputing Center, [2]Microsoft Research Cambridge, UK

The PowerPC 405 Memory Sentinel and Injection System
Mark Bucciero, John Paul Walters, Roger Moussalli, Shanyuan Gao and Matthew French
USC/ISI

Checkpoint/Restart and Beyond: Resilient High Performance Computing with FPGAs
Andrew Schmidt, Bin Huang, Ron Sass and Matt French
University of North Carolina at Charlotte, Information Sciences Institute University of Southern California

FUSE: Front-end user framework for OS abstraction of hardware accelerators
Aws Ismail and Lesley Shannon
Simon Fraser University

11:50am **Lunch** (Heritage Center)

1:20pm **Tuesday afternoon, Session 7: High-Level Synthesis and Tools**
Session Chairs: Ron Sass and Kyle Rupnow

Multilevel Granularity Parallelism Synthesis on FPGAs
[1]*Alexandros Papakonstantinou,* [2]*Yun Liang,* [1]*John Stratton,* [3]*Karthik Gururaj,* [1]*Deming Chen,* [1]*Wen-Mei Hwu and* [3]*Jason Cong*
[1]University of Illinois, Urbana Champaign, [2]Advance Digital Science Center, Illinois at Singapore, [3]University of California, Los Angeles

Synthesis of Platform Architectures from OpenCL Programs
Muhsen Owaida, Nikolaos Bellas, Konstantis Daloukas and Christos Antonopoulos
University of Thessaly

Programming Real-time Autofocus on a Massively Parallel Reconfigurable Architecture using Occam-pi
[1]*Zain ul-Abdin,* [2]*Anders Ahlander and* [1]*Bertil Svensson*
[1]Halmstad University, [2]SAAB AB

Towards Synthesis-Free JIT Compilation to Commodity FPGAs (short)
Davor Capalija and Tarek Abdelrahman
University of Toronto

Automated Placement for Parallelized FPGA FFTs (short)
[1]*Suraj Gowda,* [2]*Aaron Parsons,* [3]*Robert Jarnot and* [4]*Dan Werthimer*
[1]UC Berkeley, EECS, [2]UC Berkeley, Astronomy, [3]Jet Propulsion Laboratory, California Institute of Technology, [4]UC Berkeley Space Sciences Laboratory

Reducing the Energy Cost of Irregular Code Bases in Soft Processor Systems (short)
[1]*Manish Arora,* [1]*Jack Sampson,* [1]*Nathan Goulding-Hotta,* [2]*Jonathan Babb,* [1]*Ganesh Venkatesh,* [1]*Michael Taylor and* [1]*Steven Swanson*
[1]University of California, San Diego, [2]Massachusetts Institute of Technology

Extending Force-directed Scheduling with Explicit Parallel and Timed Constructs for High-level Synthesis (short)
Rohit Sinha and Hiren Patel
University of Waterloo

2:40pm **Poster Session III**

3:40pm **Tuesday afternoon, Session 8: Applications II**
Session Chair: Gordon Brebner

String Matching in Hardware using the FM index
Edward Bryann Fernandez, Walid Najjar and Stefano Lonardi
University of California Riverside

Accelerating Phylogeny-Aware Short DNA Read Alignment with FPGAs
Nikolaos Alachiotis, Simon Berger and Alexandros Stamatakis
Heidelberg Institute for Theoretical Studies

Scalable Streaming-Array of Simple Soft-Processors for Stencil Computations with Constant Memory-Bandwidth
Kentaro Sano, Yoshiaki Hatsuda and Satoru Yamamoto
Tohoku University

Memory-Efficient IPv4/v6 Lookup on FPGAs Using Distance-Bounded Path Compression
Hoang Le, Weirong Jiang and Viktor Prasanna
USC

5:00pm **Awards and Summary**

5:15pm