Security and Privacy Concerns for the FPGA-Accelerated Cloud and Datacenters

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Overview

- **Background**
  - FPGAs in the cloud
  - Multi-tenant FPGAs
  - FPGA voltage attack approaches

- **Characterizing voltage attacks on Arria 10**
  - Experimental approach
  - Characterization test results
  - Fault induction

- **RSA attack using power fluctuation on Cyclone V and Arria 10**
  - Induce delay faults in RSA
  - Use Chinese remainder theorem to extract key
Multi-Tenant FPGA

- Shared (multi-tenant) FPGAs
  - Devices are expensive. Desire to fully use resources
- Cloud computing: target for multi-tenant FPGAs?
  - Why not use partial reconfiguration?
  - User has no idea what “neighbor” is doing (side channels)
  - Don’t want to risk leaking information
- Need to understand vulnerabilities
  - Previous: temperature, voltage
  - This work: no physical access needed

Source: Intel

1 Stratix V FPGAs: Built for Bandwidth, Intel Corporation, 2010
Example: AmorphOS for Amazon EC2 F1

- Multiple users deploy circuits (Morphlets) on FPGA
- Virtualizing software multiplexing software and memory interfaces
- Attempt to create “virtual machine” like environment on the FPGA
- Increase income level for hardware use.
- Security?: not really a focus

Source: Khawaja et al\(^\text{1}\)

\(^{1}\) A. Khawaja et al., Sharing, Protection, and Compatibility for Reconfigurable Fabric with AmorphoS, OSDI, Oct. 2018
What Type of FPGA Voltage Attacks are Possible?

- On-chip voltage sensors to extract encryption key
  - Ring oscillators used to extract RSA key¹
  - Time-to-digital converters used to extract AES key²

- Voltage fluctuation-based communication
  - Communication on single FPGA³,⁴

- On-chip voltage supply attacks
  - Induce stealthy faults⁵, ⁶, ⁷

- Drive FPGA into reset⁷

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¹ Zhao and Kuh, FPGA-Based Remote Power Side-Channel Attacks, IEEE Symp. Security and Privacy, May 2018
² Schellenberg et al, An Inside Job: Remote Power Analysis Attacks on FPGAs, DATE, March 2018
⁴ Giechaskiel et al., “Reading between the dies: Cross-SLR covert channels on multi-tenant cloud FPGAs“ ICCD, Oct. 2019
⁵ Krautter et al, FPGAhammer: Remote Voltage Fault Attacks on Shared FPGAs, suitable for DFA on AES, CHES, vol 3 , 2018
⁶ Mahmoud and Stojilovic, “Timing violation induced faults in multi-tenant FPGAs,” in DATE 2019
⁷ Provelengios, “Characterizing Power Distribution Attacks in Multi-User FPGA Environments”, FPL 2019
Overview

- Two tenants are using simultaneously the device
- Tenant A (attacker) consumes power aggressively in an attempt to induce timing faults in tenant B (victim)

Threat model:
- Tenants are spatially isolated but share the FPGA power distribution network (PDN)
- Tenants do not have physical access to the board
- The tools used for interacting with the FPGA are secure
Contribution

- We investigate on-chip voltage attacks and specifically how their impact depends on:
  - Duration of voltage disruption
  - Consumed power by attacker
  - Distance between attacker & victim

- We evaluate the ability of power wasting circuits to induce timing faults to victim

- We examine the ability of power wasting circuits to reveal an RSA encryption key through fault injection
Voltage sensor architecture

- A regular rectangular grid of 46 sensors
- 19 inverting stages:
  - Meet timing constraints
  - Minimize local effects
  - Fit in a single CV LAB
- Arria 10 parameters
  - $f_{RO} = 150$ MHz
  - Samp. period = 10µs

Controller reads and resets all the sensors simultaneously in every sampling period

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Attacker circuitry

- \( P_{dyn} = C \times V_{DD}^2 \times f_{sw} \)
- 1-stage ROs as power wasters
- Arria 10: 11,424 LABs fit up to 28K PW
- Placed uniformly at random locations in the attack area

<table>
<thead>
<tr>
<th>Number of Instances</th>
<th>Power / Inst. [mW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>12k</td>
<td>2.17</td>
</tr>
<tr>
<td>16k</td>
<td>2.18</td>
</tr>
<tr>
<td>20k</td>
<td>2.21</td>
</tr>
<tr>
<td>24k</td>
<td>2.18</td>
</tr>
<tr>
<td>28k</td>
<td>2.20</td>
</tr>
</tbody>
</table>
Arria 10 sensor calibration

- To use ROs as on-chip voltage sensors:
  - Vary power waster count between 8,000 and 28,000 and record:
    - Voltage on on-chip sensor
    - RO counts from on-chip sensors

- Minimize the power drawn by the FPGA during measurements

![Graph showing normalized frequency vs. voltage](image)
Voltage drop characterization in Arria 10

- Evaluate the Arria 10 PDN response
- 28k RO-based PW instances
- 12 on-chip sensors at different distances to the center of the waster
- Peak voltage drop ~8us after activating PWs
Characterizing timing faults

- Voltage drop causes delay of combinational logic to increase
- Wrong values captured if paths do not complete before capturing clock edge arrives
- Must overcome conservative timing models
- Use ripple carry adder as a representative test circuit which allows us to sensitize various path lengths
Arria 10 timing faults

- 28k PWs randomly placed in an area of 11,424 LABs (168x68)
- Steep voltage drop at 20 ns induces faults
- Faults peak at 8 µs
- Substantially fewer faults than Cyclone V
Can a victim evade the attack?

- In Arria 10, the initial fast voltage drop is not location dependent.
- Faults from legal paths reported even at the edge of the device.
Mapping the Arria 10 voltage drop

- Using 132 on-chip sensors for deriving the voltage contours
- Varying the magnitude of disturbance and location of attacker
- Center of attack:
  - 28K PWs: 767mV
  - 8K PWs: 862mV
- Upper right corner of the chip:
  - 28K PWs: 797mV

(A) 28K power waster attack
(B) 8K power waster attack
Locating the Arria 10 attack area

- The disturbance of the shared PDN reveals the location of the attacker
- Evaluate how many sensors required to find its location
- 64 sensors are sufficient to identify the attacker

Resource utilize.: Arria 10AX115N2F45E1SG

<table>
<thead>
<tr>
<th>Num. RO Sensors</th>
<th>ALMs (Avail.: 427,200)</th>
<th>Flip-flops (Avail.: 1,708,800)</th>
</tr>
</thead>
<tbody>
<tr>
<td>64</td>
<td>1,280 (&lt;1%)</td>
<td>1,280 (&lt;1%)</td>
</tr>
<tr>
<td>132</td>
<td>2,640 (&lt;1%)</td>
<td>2,640 (&lt;1%)</td>
</tr>
<tr>
<td>Controller</td>
<td>1,008 (&lt;1%)</td>
<td>134 (&lt;1%)</td>
</tr>
</tbody>
</table>

(A) 28K power waster attack

(B) 8K power waster attack
12 ring oscillators located in middle of device
- 10,000 power wasters
- Sampling period of 10 µs
- Ongoing: translating RO count to voltage
Attacking RSA through fault injection

- Exploiting the use of the Chinese Remainder Theorem (CRT) \(^1\):

<table>
<thead>
<tr>
<th>Direct RSA</th>
<th>RSA with CRT (4x faster)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( Y = X^e \mod N )</td>
<td>( Y = aY_1 + bY_2 )</td>
</tr>
<tr>
<td></td>
<td>( Y_1 = (X \mod p)^e \mod (p-1) \mod p )</td>
</tr>
<tr>
<td></td>
<td>( Y_2 = (X \mod q)^e \mod (q-1) \mod q )</td>
</tr>
</tbody>
</table>

- **Goal:** Inject fault(s) while computing \( Y_1 \) or \( Y_2 \)

- **Fault during CRT reveals key**
  - Output \( Y \) is assembled with a faulty \( Y_1 \)
  - Prime number \( q \) is revealed
  - Private key \( e \) can be reconstructed
  - \( e \) can also be extracted with a faulty \( Y_2 \)

  ➢ The attack works for any key length
  ➢ A single interaction is sufficient \(^2\)

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\(^1\) D. Boneh et al., On the Importance of Eliminating Errors in Cryptographic Computations, Journal of Cryptology, 2001

\(^2\) A.K Lenstra, Memo on RSA signature generation in the presence of faults, 1996
RSA experimental setup

- 128-bit RSA implementation is placed in an area of 256 LABs
- Wasters are placed at random locations around the RSA core covering an area of 1,940 LABs
- A script running on host PC is responsible for controlling the experiment

Resource utilization: Cyclone V 5CSEMA5F31C6

<table>
<thead>
<tr>
<th>RSA core</th>
<th>ALMs (Avail.: 32,070)</th>
<th>Flip-flops (Avail.: 128,280)</th>
<th>Memory [Kb] (Avail.: 3,970 Kb)</th>
<th>F_max [MHz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>128-bit</td>
<td>1,236 (3.9%)</td>
<td>1,925 (1.5%)</td>
<td>16</td>
<td>94.74</td>
</tr>
</tbody>
</table>

(Quartus Prime 17.1 - ChipPlanner)
Extracting the RSA private key

- Hardware computes $Y_1$ and $Y_2$ while wasters are turned on
- Reading out $Y_1$, $Y_2$ and assembling final output $Y$
- $Y$ does not match the expected output
- Extract the first prime
- Factor $N$ to get the second prime
- Reconstruct the private exponent
- Extracted and original keys match

```bash
lab@lab:/project/$ make rsa_attack B-builds/build_2020-02-15_04-48-53
Resetting RSA core and setting test parameters ...
Starting experiment ...
Turn on 10080 wasters at time 0.00800183
Waiting for 1 seconds ... 1, done
[mif_parser] parsing extracted MIF and dumping to file(s) ... done
Retrieving Y1 and Y2 RSA outputs ... done
******** Test Completed ********
RSA test : FAIL
Key length : 128 bit

RSA core output: 0x35f3ad9c676ffcedbd2b5d621ed718b9
Expected output: 0x34bc3c66590eaf60fcb488411e3f0bea2

[extract_rsakey] RSA output: 0x35f3ad9c676ffcedbd2b5d621ed718b9
[extract_rsakey] Extract the first prime number using the faulty output (p1 - gcd(x - y^pub exp, N)): p1 - 0x8cabcc4e903eall1
[extract_rsakey] Factor modulus N (p2 - N/p1) to get the second prime number: p2 - 0x653790eb1b036bd
[extract_rsakey] Calculate phi ((p1-1)*(p2-1)): phi - 0x7884d7f6471889a7e87ffaba9f7a7c0
[extract_rsakey] Calculate the priv. exponent (pr exp = (1/pub exp) mod phi): Extracted priv. exponent = 0x710c43115c59495105ea53342309a0a9

Original key: 0x710c43115c59495105ea53342309a0a9
```

Timing fault(s) occurred!
How many wasters are required?

- Vary the number of wasters and find the probability of extracting the key

- Cyclone V:
  - 11K-12K PWs: high chance of extracting the key undetected
  - $F_{\text{max}}$: 94.74MHz, $F_{\text{break}}$: 166MHz (w/o wasters)

- Identifying weak spots in Arria 10 based on:
  - Number of PWs that can safely be activated
  - Yield in less timing margin

<table>
<thead>
<tr>
<th>Loc.</th>
<th>PWs [k]</th>
<th>$F_{\text{max}}$ [MHz]</th>
<th>$F_{\text{break}}$ [MHz] (w/ wasters)</th>
<th>$F_{\text{break}}$ [MHz] (w/o wasters)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1, B1</td>
<td>20</td>
<td>179</td>
<td>250</td>
<td>270</td>
</tr>
<tr>
<td>A1, B1</td>
<td>24</td>
<td>162</td>
<td>262</td>
<td>281</td>
</tr>
<tr>
<td>A1, B1</td>
<td>28</td>
<td>165</td>
<td>240</td>
<td>268</td>
</tr>
<tr>
<td>D3, D4</td>
<td>30</td>
<td>103</td>
<td>123</td>
<td>137</td>
</tr>
</tbody>
</table>

- Work in progress

Cyclone V

- Extracting key
- Resetting board

Arria 10

- Loc.
- PWs [k]
- $F_{\text{max}}$ [MHz]
- $F_{\text{break}}$ [MHz] (w/ wasters)
- $F_{\text{break}}$ [MHz] (w/o wasters)

- Number of PWs that can safely be activated
- Yield in less timing margin

- Work in progress

~4.5ns margin!
How many wasters are required? (cont’d)

- Vary the number of wasters and find the probability of extracting the key
- 11K-12K PWs: high chance of extracting the key undetected
- \( F_{\text{max}}: 94.74\text{MHz}, F_{\text{break}}: 166\text{MHz} \) (w/o wasters)

~4.5ns margin!
Summary

- Multi-tenant FPGAs
  - Logical next step for cloud computing

- Voltage based attacks
  - Easy to create power wasting circuits that induce faults or crash FPGA

- Characterizing voltage attacks on Arria 10
  - 15% core voltage drop within 8 us
  - Induces faults throughout device

- RSA attack
  - Single fault sufficient to expose key
  - Effective for Cyclone V (even defeats built in timing margin)
  - Effective for Arria 10 if design is overclocked