Automatic High-Level Hardware Checkpoint Selection for Reconfigurable Systems

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Hardware context switch

1. Task 1
2. FPGA (task 1)
3. Memory

Bus

time

C

Task 1

C

Task 2

C

rest

Task 1

Preemption demand

Preemption demand

C: chip configuration
save: context saving
rest: context restoring
Hardware context switch

- Task 1
  - CPU
  - FPGA
  - Memory

Bus

Time

- Preemption demand
  - Task 1
  - Task 2

C: chip configuration
save: context saving
rest: context restoring
Hardware context switch

- Task 1
- Task 2
- CPU
- FPGA
- Memory
- Bus

Preemption demand

Save: context saving
Rest: context restoring

C: chip configuration
Algorithm with 2 inputs:
- FSM of the HW task
- Latency
Algorithm with 2 inputs:
- FSM of the HW task
- Latency

⇒ set of checkpoints

Circuit produced:
- Minimized area overhead
- Reduced memory footprint
- Respect preemption latency

Algorithm implemented in an HLS tool
Comparison

- Data footprint: smaller
- Design efforts: lesser
- Additional resources: fewer
- Technology independence
- Extraction time: smaller
Comparison

Data footprint
- smaller

Design efforts
- lesser

Scan-chain
- fewer

Additional resources

Extraction time

Technology independency

Readback

Our solution

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Further presentation of contributions:

- results!
  - 85% less memory elements to save
  - 52% HW overhead reduction
- more details about the method and implementation
- come and see our open source HLS tool AUGH and its plugin CP3