Technology Scaling in FPGAs

SFU

Trends in Applications and Architectures

Lesley Shannon & Veronica Cojocaru (Simon Fraser University) Cong Nguyen Dao & Philip H.W. Leong (The University of Sydney)



CELEBRATING 50 YEARS | 1965-2015

SIMON FRASER UNIVERSITY ENGAGING THE WORLD



- > First commercial FPGA was released in 1985
- > FCCM has more than 20 years of history
- > Can we learn something about progress based on past designs?

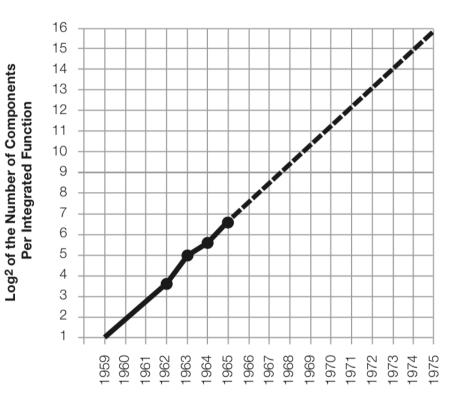


- > Develop models of area and speed across generations of FPGA devices
- See how device trends compare with those expected by Moore's Law and Dennard's Law
- > Compare performance of devices to designs published at FCCM
 - Odd years (total of 284 designs)
- > Develop model which can be used for extrapolation
 - How does this model compare using vendor cores to scale technologies?
 - How does it perform looking forward?



Moore's Law

 Gordon Moore in 1965 predicted number of transistors in an IC will double ≈ two years





- > He made the bold claim that 65,000 components could fit on an IC by 1975 (at the time they had 50)!
- > Cartoon is from the same paper





 Dennard in 1974: as transistor feature size (κ or commonly λ) decreases, power stays proportional to area

Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox} , L, W	1/к
Doping concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $\epsilon A/t$	$1/\kappa$
Delay time/circuit VC/I	$1/\kappa$
Power dissipation/circuit VI	$1/\kappa^2$
Power density VI/A	1



Device Size Table

Year	Feature Size	Xilinx FPGA	family	Device	LUTs	DSP/Mult blocks	BRAM Kbits	LUTs /DSP	LUTs /BRAM		Altera FPGA family Device		ALMs (LEs)	DSP /Mult blocks	BRAM Kbits	LEs/ DSP	LEs/ BRAM
			V	XC7V2000T	1,221,600	2,160	46,512	566	26								
2011		Virtex 7	VX	XC7VX1140T	712,000	3,600	67,680	198	11								
			VH	XC7VH870T	547,600	2,520	50,760	217	11								
	28 nm										GT	5SGTC7	622,000	512	50,000		12
2010										Stratix V	GX	5SGXBB	952,000	704	52,000		18
											GS	5SGSD8	695,000	3,926	50,000	177	14
											E	5SEEB	952,000	704	52,000	1,352	18
			LX	XC6VLX760	474,240	864	25,920	549	18								
2009		Virtex 6	SX	XC6VSX475T	297,600	2,016	38,304	148	8								
	40 nm		НХ	XC6VHX565T	354,240	864	32,832	410	11			554646665	524 222	1 00 1		510	10
										a	GT	EP4S100G5	531,200	1,024	27,376	519	19
2008										Stratix IV	GX	EP4SGX530	531,200	1,024	27,376	519	19
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			LX	XC5VLX330	207,360	192	10,368	1,080	20								
2005	65	Virtex 5	SX	XC5VSX240T	149,760	1,056	18,576	142	8								
2006	65 nm		FX	XC5VFX200T	122,880	384	16,416	320	/			50261240	227 500	576	16 272	500	21
										Stratix III		EP3SL340	337,500	576	16,272	586	21 17
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2005	90 nm									Stratix II	GX	EP2SGX130/G	132,540	252	6,747	526	20
	130 nm		LX	XC4VLX200	178,176	96	6,048	1,856	29			EP2S180	179,400	384	9,383	467	19
2004	90 nm	Virtex 4	SX	XC4VLX200 XC4VSX55	49,152	512	5,760	1,856	29								
2004	30 1111	VIILEX 4	FX	XC4VFX140	126,336	192	9,936	658	13								
			FA	704417140	120,550	192	9,930	038	15		GX	EP1SGX40D	41,250	56	3,423	737	12
2002	130 nm									Stratix	- 0^	EP1580	79,040	88	7,428	898	11
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2001	0.15 um	1	v	XC2V8000	93,184	168	3,024	555	31	Mercury		EP1M350	14,400	0	115	-	125
2000	0.18 um	l		ACLICCOU	55,201	100	5,621			Excalibur		EPXA10	38,400	0	3,146		12
1999	0.18 um			XCV3200E	64,896	0	851	-	76						-,		
	0.22 um									Flex 10KE		EPF10K200E	9,984	0	98	-	102
1998	0.25 um	Virtex		XCV1000	24,576	0	131	-	188								
1997	0.35 um	4000 E/XL		XC4085XL	12,544	0	0	-	-								
1996	0.3 um				-					Flex 10KA		EPF10K250A	12,160	0	41	-	297
1995	0.42 um	1								Flex 10K		EPF10K100	4,992	0	25	-	200
1992	0.6 um	1								Flex 8000		EPF81500A	1,296	0	0	-	-
1991	0.8um	4000 series		XC4025	2,048	0	0	-	-								
1985	2 um	2000 series		XC2018	400	0	0	-	-								



Normalising Resource Usage

How do we compare designs over process technologies:

- > 4-LUTs and 6-LUTs?
 - Altera ALM = 2.5 4-LUTs
 - Xilinx 6-LUT = 1.4 4-LUTs



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Normalising Resource Usage

How do we compare designs over process technologies:

- > Multipliers DSP/blocks
 - Altera DSP blocks counted as number of 18x18 multipliers
 - All Xilinx multipliers (whether 18x18 or 25x18) considered an 18x18 multiplier



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1996	0.33 um	4000 L/ XL		AC400JAL	12,344	0	0			Flex 10KA		EPF10K250A	12,160	0	41	_	297
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Normalising Resource Usage

How do we compare designs over process technologies:

- > Embedded memory sizes?
 - Just using number of kilobits

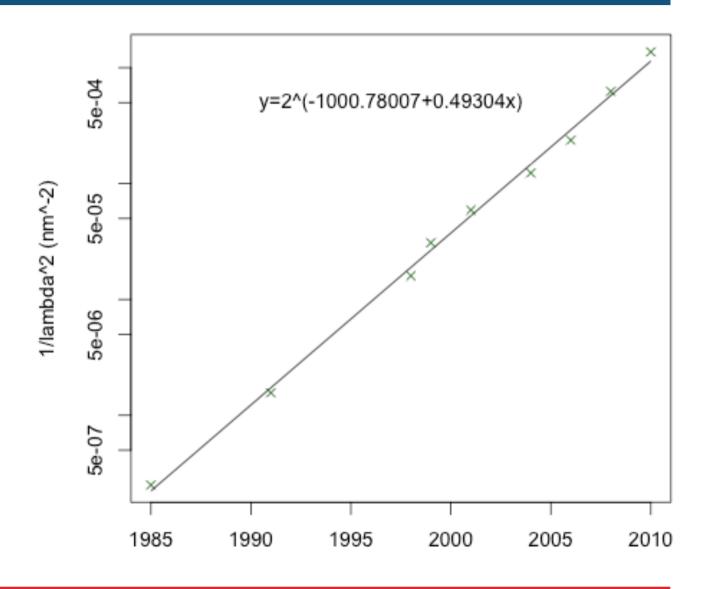


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1991	0.8um	4000 series		XC4025	2,048	0	0	-	-								
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$1/\lambda^2$ vs year

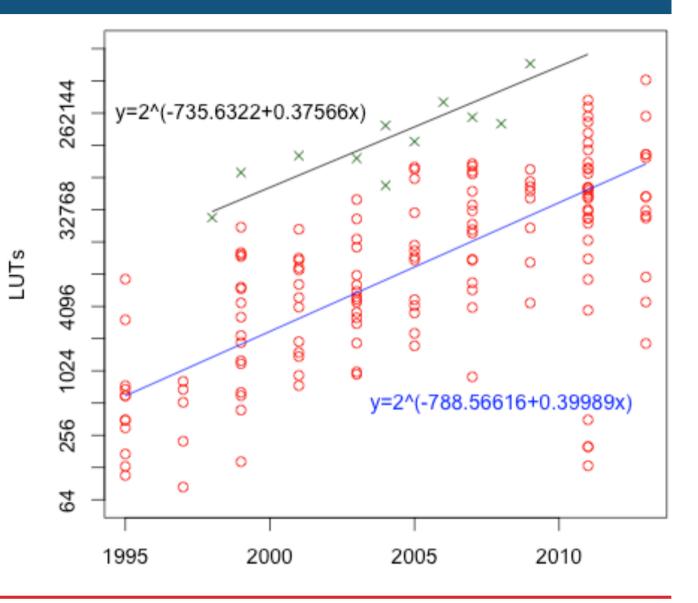
- FPGA lambda
 from previous
 table plotted vs
 year
- Transistor density doubling every two years, in agreement with Moore's Law





Design Size (number of LUTs)

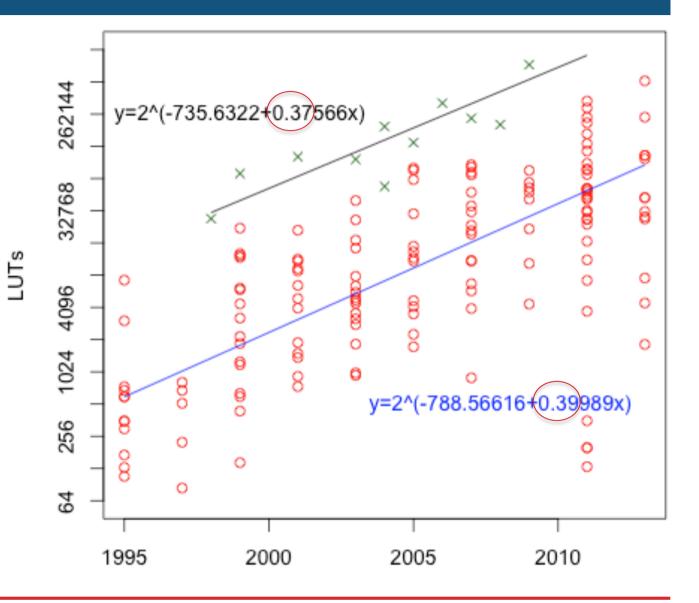
- x's are the number of LUTs in the largest FPGA of that year
- > o's are FCCM designs
- Tech design size doubles every 2.5 years (slightly slower than Moore's Law)
- Inaccuracies
 because we don't
 count clock trees
 and hard blocks





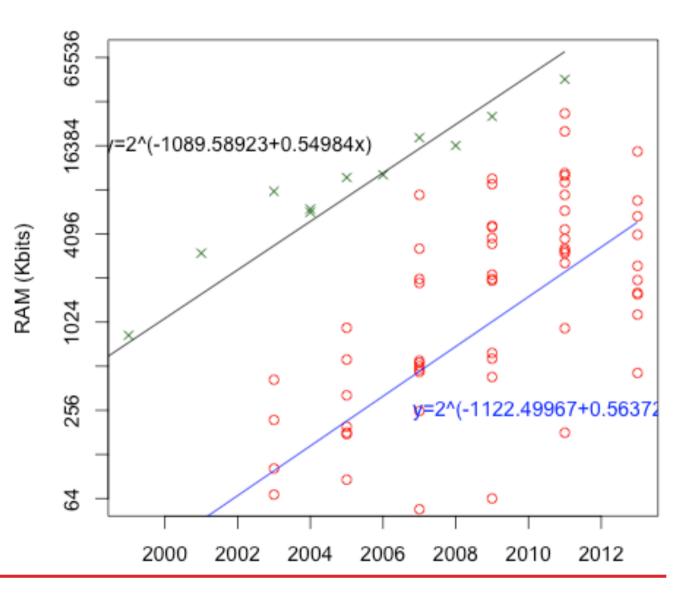
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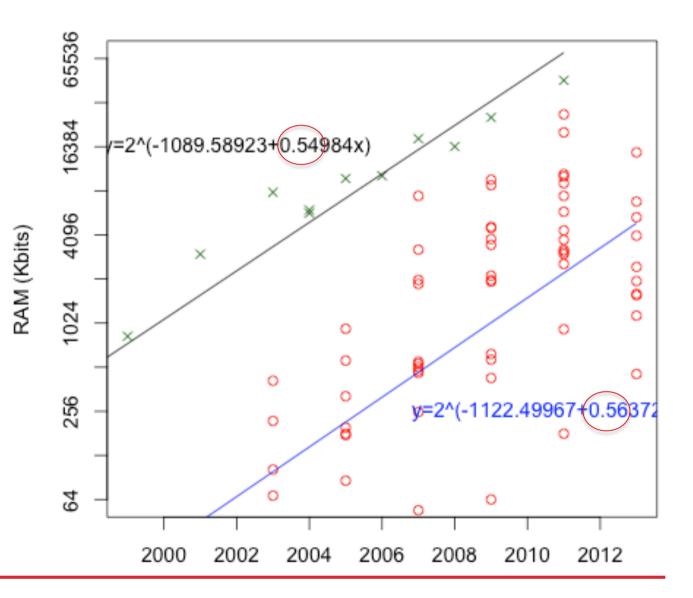
BRAM Usage

- Tech doubles every 1.8 years
- Research doubles every 1.8 years
- General trend consistent with Moore's Law



BRAM Usage

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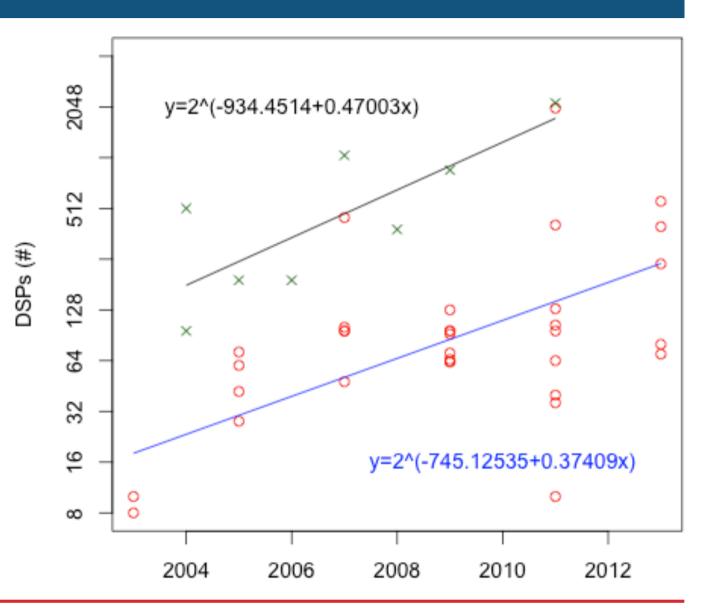
Number of DSPs

Tech trend
 consistent with
 Moore's Law

SFU

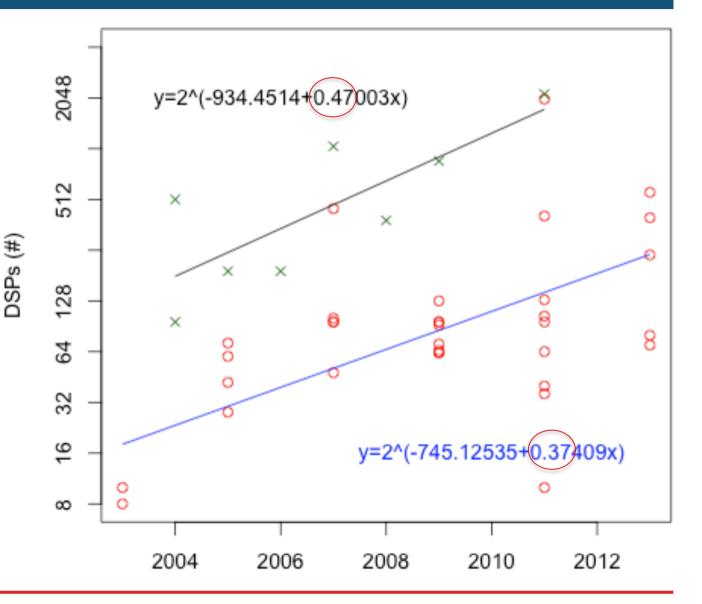
THE UNIVERSITY OF SYDNEY

- Research
 doubles every 2.6
 years (slower
 than Moore's
 Law, same rate as
 LUTs)
- In some designs
 DSPs not used or
 not limiting factor



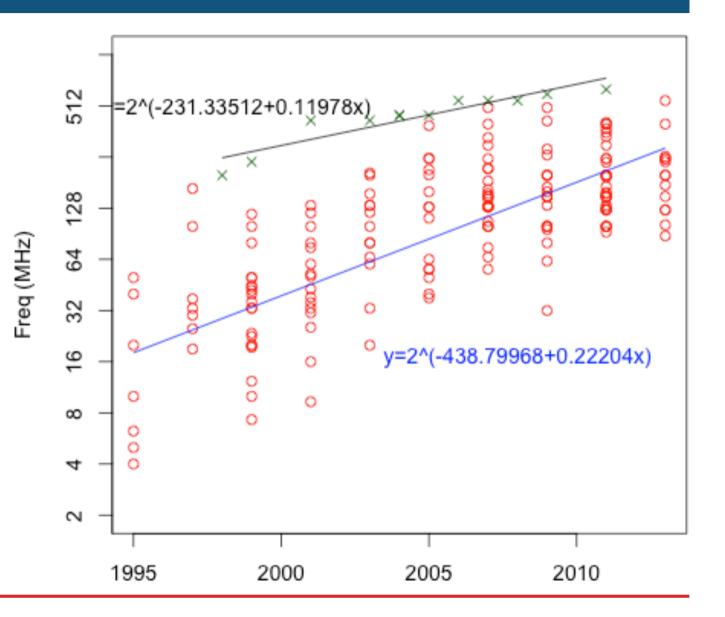
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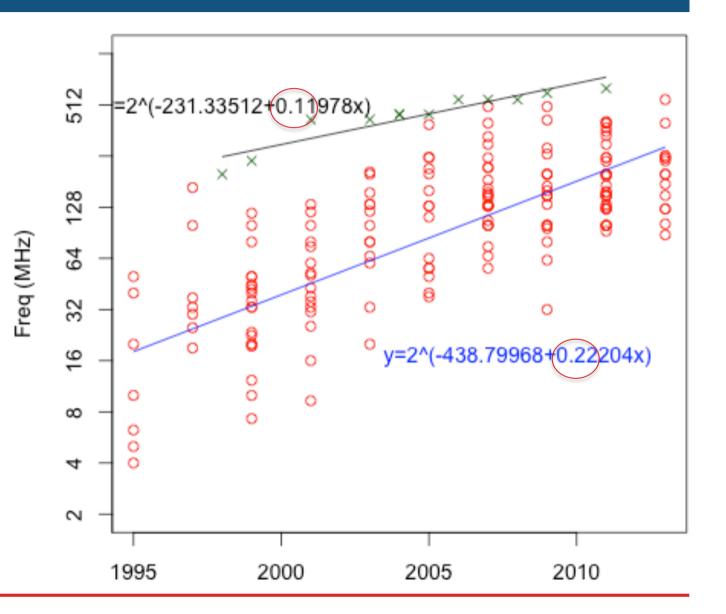
Clock Frequency

- Tech freq doubles every 8 years
- Research freq doubles every 5 years
- Expect doubling every 4 years from Dennard
- Maybe due to hard blocks pushing up frequencies



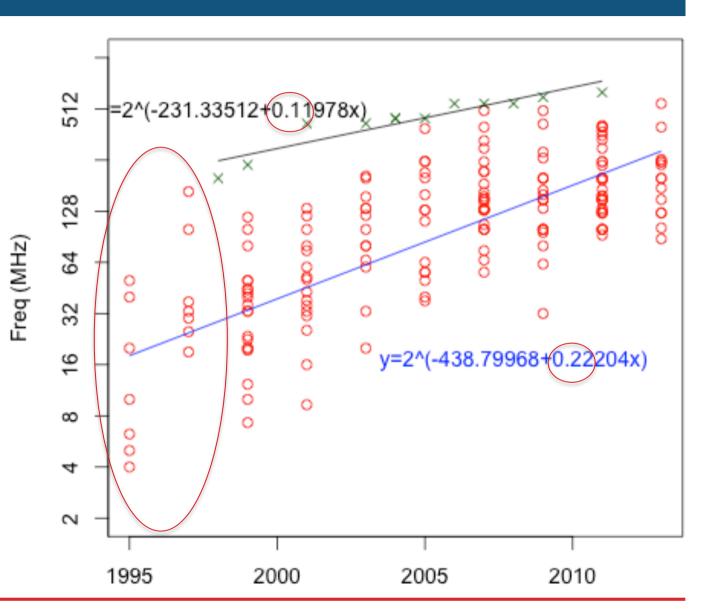
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Clock Frequency

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- Expect doubling every 4 years from Dennard
- Maybe due to hard blocks pushing up frequencies
- Note tech trends start from a high value so line is flatter



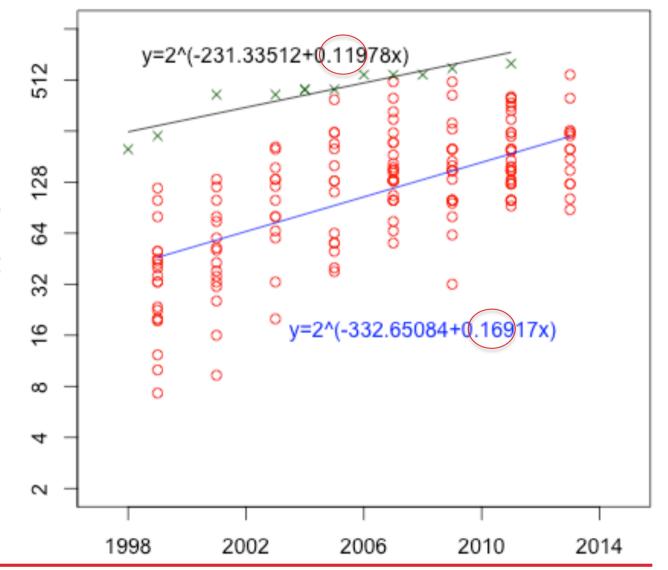


Clock Frequency (1999-2013)

- Tech freq doubles every 8 years
- Research freq doubles every <u>6</u> years

Freq (MHz)

 Tracking much better with what might be expected based on technology scaling





> How did we do for 2015?

- Sample designs are from the Applications Session

	4-LUTs (Normalised)	BRAMs (kBits)	DSPs	Operating Frequency	Operating Frequency (updated)
FCCM 2015 data from Apps session (median points)	130536	13338	420	232MHz	232MHz
Predicted	151840	10780	406	390MHz	300MHz
Relative Error (%)	16%	-19%	-3%	68%	29%



- > Quantitative study of 20 years of FCCM designs
 - FPGA feature size closely following Moore's Law
 - # lookup tables for research designs and devices doubling every 2.5 years
 - Design and device operating frequency double in 8 and 5 years respectively, slower than that offered by technology scaling
 - Memory utilization of designs and devices doubling every 1.8 years
 - # DSPs increasing at a faster rate than research designs



- > Abovementioned trends can be modeled using the equations introduced
 - In the tradition of FCCM, here's a prediction for the median number of used LUTS used in designs for 2025:

y=2^(-788.56616+0.39989 * 2025) = **2,427K**

> All data available from: <u>http://www.ee.usyd.edu.au/~phwl/UserFiles/File/misc/trends_fccm15.zip</u>

_(link also available in paper)



- > More detailed determination of normalization factors
- > Hypothesized hard blocks are a major factor but not studied
- Do similar studies for different designs, parameters and hard blocks (particularly Rent's Rule and power consumption)
- > Use information from research designs to develop better architectures
- > Compare these predictions with actual data in the future



Questions?



Thank you for listening