FCCM 2013 Final Program

The 21st Annual International IEEE Symposium on Field-Programmable Custom Computing Machines
Seattle, Washington USA April 28 -30 2013 www.fccm.org

Sunday, April 28th

12:00 PM	**Registration Opens**
1:00 - 4:00 PM	**Panel Discussion** – *Reconfigurable Computing in the Era of Dark Silicon* Eric Chung (Microsoft Research) chairs this discussion regarding how the FPGA community can react to the realities of dark silicon. The panel will feature: •Doug Burger (Microsoft Research) •Mike Butts (Compute Forest) •Jan Gray (Gray Research LLC) •Chuck Thacker (Microsoft Research) •Kees Vissers (Xilinx) •John Wawrzynek (UC Berkeley)
4:00 - 6:00 PM	**Pico Computing Workshop** This tutorial describes Pico Computing's vision for simplifying FPGA development. Pico provides an FPGA framework and a flexible software API that eliminates the typical boilerplate required to develop accelerated applications and/or perform architectural exploration. This workshop will walk users through the Pico framework and development cycle, demonstrating both the software and HDL required to migrate a compute-intensive software application to an accelerated software/hardware solution.
6:00 – 8:00 PM	**Welcome Reception** – Sponsored by Pico Computing Come relax with your colleagues over drinks and light hors d'oeuvres.

Monday, April 29th

8:00 AM	**Registration Opens**
8:00 - 9:00 AM	**Continental Breakfast**
9:00 AM	**Opening Remarks by Ken Eguro and Miriam Leeser**
9:10 AM	**Session 1: Data Driven Computing** — **Session Chair – Mike Wirthlin**
9:10 AM	*Parallel Computation of Skyline Queries* Louis Woods[1], Gustavo Alonso[1], and Jens Teubner[2] [1]ETH Zurich, [2]TU Dortmund University
9:30 AM	*Minerva: Accelerating Data Analysis in Next-Generation SSDs* Arup De[12], Maya Gokhale[2], Rajesh Gupta[1], and Steven Swanson[1] [1]University of California, San Diego, [2]Lawrence Livermore National Laboratory
9:50 AM	*Accelerating Join Operation for Relational Databases with FPGAs (short)* Robert Halstead[1], Bharat Sukhwani[2], Hong Min[2], Mathew Thoennes[2], Parijat Dube[2], Sameh Asaad[2], and Balakrishna Iyer[3] [1]University of California Riverside, [2]IBM T. J. Watson Research Center, [3]IBM Silicon Valley Lab
9:55 AM	*Boosting Memory Performance of Many-Core FPGA Device through Dynamic Precedence Graph (short)* Yu Bai, Abigail Fuentes, Michael Riera, Mohammed Alawad, and Mingjie Lin University of Central Florida
10:00 AM	*Acceleration of SQL Restrictions and Aggregations through FPGA-based Dynamic Partial Reconfiguration (short)* Christopher Dennl, Daniel Ziener, and Jürgen Teich University of Erlangen-Nuremberg

10:05 AM	**Poster Session I and Coffee Break** — **Session Chair – Justin Tripp**

Binding Hardware IPs to Specific FPGA Device via Inter-twining the PUF Response with the FSM of Sequential Circuits

Jiliang Zhang[12], Yaping Lin[1], Yongqiang Lu[2], Ray C.C. Cheung[3], Wenjie Che[1], Qiang Zhou[2], and Jinian Bian[2]

[1]Hunan University, [2]Tsinghua University, [3]City University of Hong Kong

A Delay-based PUF Design Using Multiplexers on FPGA

Miaoqing Huang and Shiming Li

University of Arkansas

A Configurable Architecture for a Visual Saliency system and its Application in Retail

Nandhini Chandramoorthy, Siddharth Advani, Kevin Irick, and Vijaykrishnan Narayanan

Pennsylvania State University

Global Atmospheric Simulation on a Reconfigurable Platform

Lin Gan[1], Haohuan Fu[1], Wayne Luk[2], Chao Yang[3], Wei Xue[1], and Guangwen Yang[1]

[1]Tsinghua University, [2]Imperial College London, [3]Chinese Academy of Sciences

FPGA Simulation Engine for Customized Construction of Neural Microcircuit

Jason Cong, Hugh T. Blair, and Di Wu

University of California, Los Angeles

The Impact of Hardware Communication on a Heterogeneous Computing System

Shanyuan Gao, Bin Huang, and Ron Sass

University of North Carolina at Charlotte

A Fast and Accurate FPGA-Based Fault Injection System

Thomas Schweizer, Dustin Peterson, Johannes Maximilian Kuehn, Tommy Kuhn, and Wolfgang Rosenstiel

Eberhard Karls Universität Tübingen

PLUS POSTERS FOR SHORT PAPERS FROM PAPER SESSION 1

11:15 AM	**Session 2: Hardware Considerations** — **Session Chair – Jason Anderson**

11:15 AM *Accuracy-Performance Tradeoffs on an FPGA Through Overclocking*

Kan Shi, David Boland and George A. Constantinides

Imperial College London

11:35 AM *Safe Overclocking in Tightly Coupled Processor Arrays*

Alex Brant, Ameer Abdelhadi, Douglas Sim, Tom Tang, Michael Yue, and Guy G.F. Lemieux

University of British Columbia, Vancouver

11:55 AM *Escaping the Academic Sandbox: Realizing VPR Circuits on Xilinx Devices*

Eddie Hung, Fatemeh Eslami, and Steven J. E. Wilton

University of British Columbia, Vancouver

12:15 PM *A Case for Heterogeneous Technology-Mapping: Soft versus Hard Multiplexers (short)*

Madhura Purnaprajna and Paolo Ienne

Ecole Polytechnique Fédérale de Lausanne (EPFL)

12:20 PM *Accurate Thermal-Profile Estimation and Validation for FPGA-Mapped Circuits (short)*

Abdulazim Amouri, Hussam Amrouch, Thomas Ebi, Jörg Henkel, and Mehdi Tahoori

Karlsruhe Institute of Technology (KIT)

12:25 PM	*On-chip Context Save and Restore of Hardware Tasks on Partially Reconfigurable FPGAs (short)* Aurelio Morales-Villanueva and Ann Gordon-Ross University of Florida, Gainesville
12:30 PM	**Lunch**
2:00 PM	**Session 3: Applications I** — **Session Chair – Matthew French**
2:00 PM	*A High Throughput No-Stall Golomb-Rice Hardware Decoder* Roger Moussalli, Walid Najjar, Xi Luo, and Amna Khan University of California Riverside
2:20 PM	*Image Segmentation Using Hardware Forest Classifiers* Neil Pittman[1], Alessandro Forin[1], Antonio Criminisi[2], Jamie Shotton[2], and Atabak Mahram[3] [1]Microsoft Research Redmond, [2]Microsoft Research Cambridge, [3]Boston University
2:40 PM	*A Reconfigurable Architecture for 1-D and 2-D Discrete Wavelet Transform (short)* Qing Sun, Jiang Jiang, Yongxin Zhu, and Yuzhuo Fu Shanghai Jiao Tong University
2:45 PM	*High Speed Video Processing Using Fine-Grained Processing on FPGA Platform (short)* Zhi Ping Ang, Akash Kumar, and Yajun Ha National University of Singapore
2:50 PM	**Poster Session II and Coffee Break**
	Posters for short papers from Paper Sessions 2 and 3
3:50 PM	**Session 4: Tools** — **Session Chair – Suhaib A. Fahmy**
3:50 PM	*The Effect of Compiler Optimizations on High-Level Synthesis for FPGAs* Qijing Huang, Ruolong Lian, Andrew Canis, Jongsok Choi, Ryan Xi, Stephen Brown and Jason Anderson University of Toronto
4:10 PM	*Automating Elimination of Idle Functions by Run-Time Reconfiguration* Xinyu Niu[1], Thomas Chau[1], Qiwei Jin[1], Wayne Luk[1] and Qiang Liu[2] [1]Imperial College London, [2]Tianjin University
4:30 PM	*Open-Source Bitstream Generation* Ritesh Kumar Soni[12], Neil Steiner[2], and Matthew French[2] [1]Virginia Tech, [2]University of Southern California – Information Sciences Institute
4:50 PM	*ShrinkWrap: Compiler-Enabled Optimization and Customization of Soft Memory Interconnects (short)* Eric Chung[1] and Michael Papamichael[2] [1]Microsoft Research, [2]Carnegie Mellon University
4:55 PM	*PRML: A Modeling Language for Rapid Design Exploration of Partially Reconfigurable FPGAs (short)* Rohit Kumar and Ann Gordon-Ross University of Florida, Gainesville
6:00 PM	**Demo Night Banquet** This informal show-and-tell over dinner and drinks is a long standing and exciting FCCM tradition. This is a great opportunity to discuss your work with attendees in a relaxed setting! During the event, we will also take time to honor 20 years of FCCM by presenting awards to the authors and papers selected to appear in our FCCM20 highlights volume – a special-edition proceedings containing the most significant papers presented at the conference through the years.

Tuesday, April 30th

8:00 AM	**Registration Opens**
8:00 - 9:00 AM	**Solarflare University Program Breakfast** Start your day right with Solarflare's Breakfast Reception! Learn about Solarflare's new University Program that provides FPGA-based products for classroom instruction in Computer Science and Computer Engineering and enables Computer Science researchers to pioneer advances in Custom Compute through the use of Solarflare's AOE (ApplicationOnload Engine) hardware and development kits. For more information on Solarflare's University Program, please visit http://www.solarflare.com/University-Program
9:00 AM	**Session 5: Networking** — **Session Chair – Gordon Brebner**
9:00 AM	*Atacama: An Open FPGA-based Platform for Mixed-Criticality Communication in Multi-Segmented Ethernet Networks* Gonzalo Carvajal[1], Miguel Figueroa[1], Robert Trausmuth[2], and Sebastian Fischmeister[3] [1]Universidad de Concepcion, [2]UAS Technikum Wien, [3]University of Waterloo
9:20 AM	*Latency-Optimized Networks for Clustering FPGAs* Trevor Bunker and Steven Swanson University of California, San Diego
9:40 AM	*A Range and Scaling Study of an FPGA-based Digital Wireless Channel Emulator* Scott Buscemi[1], Will Kritikos[2], and Ron Sass[2] [1]SPAWAR Systems Center Atlantic, [2]University of North Carolina at Charlotte
10:00 AM	*Enabling Hardware Exploration in Software-Defined Networking: A Flexible, Portable OpenFlow Switch (short)* Asif Khan[1] and Nirav Dave[2] [1]MIT – CSAIL, [2]SRI International
10:05 AM	*An FPGA based PCIE Root Complex Architecture for Standalone SOPCs (short)* Yingjie Cao[1], Yongxin Zhu[1], Xu Wang[1], Jiang Jiang[1], and Meikang Qiu[2] [1]Shanghai Jiaotong University, [2]University of Kentucky
10:10 AM	**Poster Session III and Coffee Break** — **Session Chair – Mike Butts**
	A Multithreaded VLIW Soft Processor Family Kalin Ovtcharov, Ilian Tili, and J. Gregory Steffan University of Toronto Exploring manycore multinode systems for irregular applications with FPGA prototyping Marco Ceriani[1], Simone Secchi[2], Antonino Tumeo[3], Oreste Villa[3], and Gianluca Palermo[1] [1]Politecnico di Milano, [2]Università di Cagliari, [3]Pacific Northwest National Laboratory Memory Access Scheduling on the Convey HC-1 Zheming Jin and Jason D. Bakos University of South Carolina An Approach to a Fully Automated Partial Reconfiguration Design Flow Kizheppatt Vipin and Suhaib A. Fahmy Nanyang Technological University An Evaluation of High-Performance Embedded Processing on MPPAs Zain-ul-Abdin and Bertil Svensson Halmstad University

	A Soft Coarse-Grained Reconfigurable Array Based High-level Synthesis Methodology: Promoting Design Productivity and Exploring Extreme FPGA Frequency Cheng Liu, Colin Lin Yu, and Hayden Kwok-Hay So The University of Hong Kong PLUS POSTERS FOR SHORT PAPERS FROM PAPER SESSIONS 4 AND 5
11:20 AM	**Session 6: Applications II** **Session Chair – Nachiket Kapre**
11:20 AM	*Application Composition and Communication Optimization of Iterative Solvers using FPGAs* Abid Rafique[1], Nachiket Kapre[2], and George Constantinides[1] [1]Imperial College London, [2]Nanyang Technological University
11:40 AM	*Parallel generation of Gaussian random numbers using the Table-Hadamard transform* David Thomas Imperial College London
12:00 PM	*Hardware-Software Codesign for Embedded Numerical Accelerators (short)* Ranko Sredojevic, Andrew Wright, and Vladimir Stojanovic MIT
12:05 PM	*FAssem : FPGA based Acceleration of De Novo Genome Assembly (short)* Sharat Chandra Varma Bogaraju[1], Paul Kolin[1], M Balakrishnan[1], and Dominique Lavenier[2] [1]Indian Institute of Technology Delhi, [2]IRISA / INRIA
12:10 PM	*Accelerating the Computation of Induced Dipoles for Molecular Mechanics with Dataflow Engines (short)* Frederico Pratas[12], Diego Oriato[2], Oliver Pell[2], Ricardo Mata[3], and Leonel Sousa[1] [1]NESC-ID/IST, [2]Maxeler Technologies, [3]Institut für Physikalische Chemie
12:15 PM	**Lunch**
1:45 PM	**Session 7: Arithmetic** **Session Chair – Kyle Rupnow**
1:45 PM	*On Optimizing the Arithmetic Precision of MCMC Algorithms* Grigorios Mingas, Farhan Rahman, and Christos-Savvas Bouganis Imperial College London
2:05 PM	*Exploiting Input Parameter Uncertainty for Reducing Datapath Precision of SPICE Device Models* Nachiket Kapre Nanyang Technological University
2:25 PM	*Efficient Large Integer Squarers on FPGA (short)* Simin Xu[1], Suhaib A Fahmy[2], and Ian V McLoughlin[2] [1]Xilinx Asia Pacific, [2]Nanyang Technological University
2:30 PM	*Elementary Function Implementation with Optimized Sub Range Polynomial Evaluation (short)* Martin Langhammer and Bogdan Pasca Altera European Technology Centre
2:35 PM	*High-Level Description and Synthesis of Floating-Point Accumulators on FPGA (short)* Marc-Andre Daigneault and Jean Pierre David Ecole Polytechnique de Montral
2:40 PM	**Poster Session IV and Coffee Break**
	Posters for short papers from Paper Sessions 6 and 7
3:40 PM	**Session 8: Applications III** **Session Chair – Ron Sass**
3:40 PM	*Reconfigurable Acceleration of Short Read Mapping* James Arram[1], Kuen Hung Tsoi[1], Wayne Luk[1], and Peiyong Jiang[2] [1]Imperial College London, [2]The Chinese University of Hong Kong

4:00 PM	*An FPGA-Based Data Flow Engine For Gaussian Copula Model* Huabin Ruan[1], Xiaomeng Huang[1], Haohuan Fu[1], Guangwen Yang[1], Wayne Luk[2], Sebastien Racaniere[3], Oliver Pell[3], and Wenjing Han[4] [1]Tsinghua University, [2]Imperial College London, [3]Maxeler Technologies, [4]Harbin Institute of Technology
4:20 PM	**Wrap Up and Best Paper Awards**